AK4311

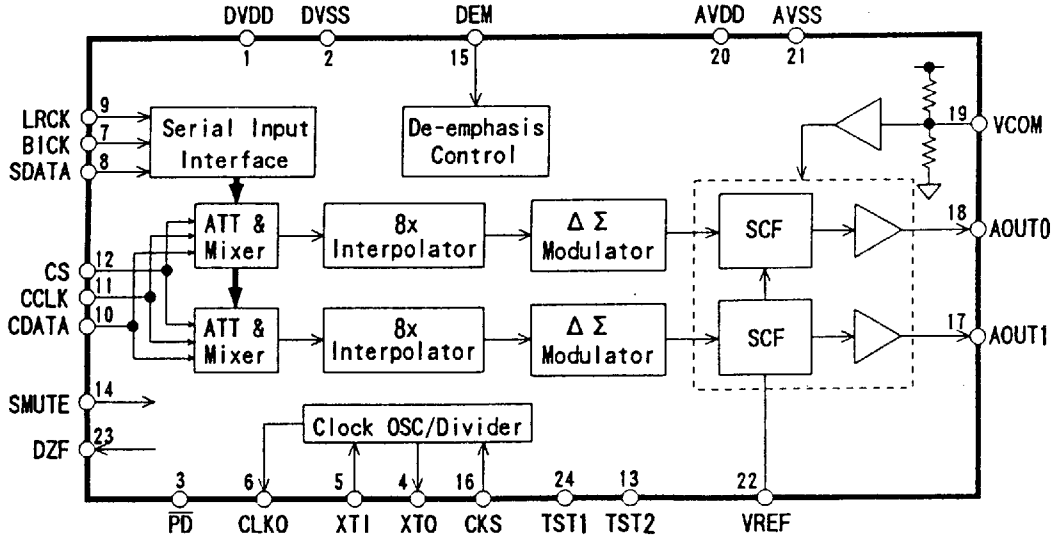
16Bit Δ Σ DAC with Volume & Mixing Control

General Description

The AK4311 is a 1bit stereo DAC with individually controllable channel volume for multimedia audio system. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4311, the loss of accuracy from clock jitter is also improved by using SCF techniques for on-chip post filter. The AK4311 includes continuos time filter with single end output and does not need any external parts. The AK4311 also has channel mixing function and meets ATAPI CD-ROM specification.

Features

- ☐ 1bit Δ Σ DAC
- ☐ Sampling Rate Ranging from 10kHz to 50kHz
- ☐ On chip Perfect filtering
  - 8 times FIR Interpolator
  - 2nd order SCF
  - 2nd order CTF
  - Total Response: ± 0.5dB at 20kHz
- ☐ On chip Buffer with Single End Output
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ On chip Individually controllable Channel Volume & Mixing Control
- ☐ Soft Mute
- ☐ Master Clock: 256fs or 384fs
- ☐ High Tolerance to Clock Jitter
- ☐ THD+N: -86dB
- ☐ Dynamic Range: 92dB
- ☐ Wide Voltage Operation: 3V ~ 5.5V
- ☐ Small Package: 24pin SSOP

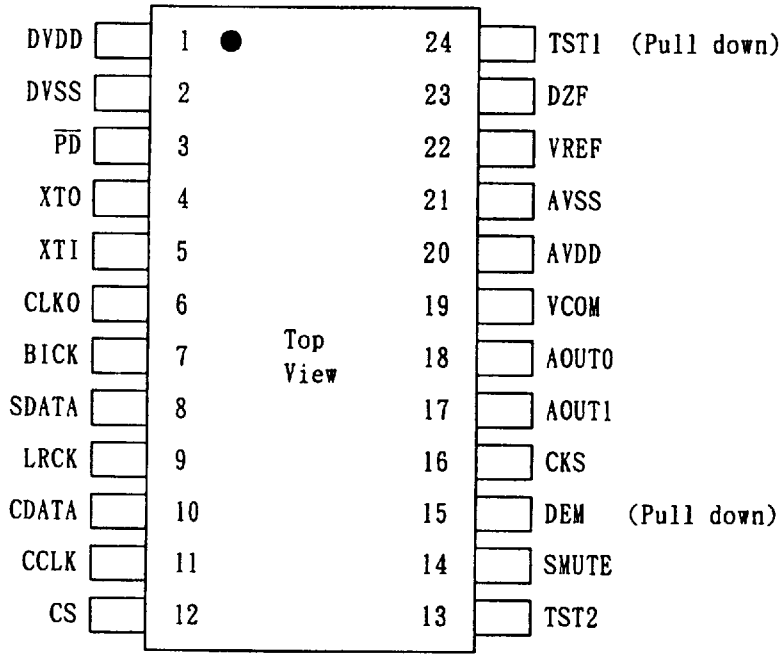


ASAHI KASEI

■ Ordering Guide

AK4311-VM	-10～+70°C	24pin SSOP(0.65mm pitch)
AKD4311	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply Pin
2	DVSS	-	Digital Ground Pin
3	$\overline{PD}$	I	Power-Down Pin When at "L", the AK4311 is in power-down mode and is held in reset. The AK4311 should always be reset upon power-up.
4	XTO	O	Crystal Oscillator Output Pin When an external clock is input, this pin should be left floating.
5	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI.
6	CLKO	O	Clock Buffer Output Pin An inverting clock of XTI is output from this pin.
7	BICK	I	Serial Bit Input Clock Pin This clock is used to latch audio data.
8	SDATA	I	Audio Data Input Pin 2's complement MSB-first data is input on this pin.
9	LRCK	I	L/R Clock Pin This input determines which audio channel is currently being input on SDATA pin. "H": Lch, "L": Rch
10	CDATA	I	Control Data Input Pin
11	CCLK	I	Control Clock Input Pin
12	CS	I	Chip Select Pin
13	TST2	O	Test Pin Must be left floating.
14	SMUTE	I	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated.
15	DEM	I	De-emphasis Enable Pin (Pull-down pin) When "H", De-emphasis of fs=44.1kHz is enabled.
16	CKS	I	Master Clock Select Pin "L": CLK=256fs, "H": CLK=384fs
17	AOUT1	O	Ch1 Analog Output Pin
18	AOUT0	O	Ch0 Analog Output Pin
19	VCOM	O	Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
20	AVDD	-	Analog Power Supply Pin
21	AVSS	-	Analog Ground Pin
22	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and AVSS set the analog output range. Normally connected to AVSS with a 0.1uF ceramic capacitor.
23	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".
24	TST1	I	Test Pin (Pull-down pin) Must be left floating or tied to AVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog (AVDD pin)	AVDD	-0.3	6.0	V
	Digital (DVDD pin)	DVDD	-0.3	AVDD+0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage		VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature		Ta	-10	70	℃
Storage Temperature		Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies: Analog (AVDD pin)		AVDD	3.0	5.0	5.5	V
Digital (DVDD pin)		DVDD	3.0	5.0	AVDD	V
AVDD-DVDD	(Note 2)	ΔVDD	0.0	-	1.0	V
Voltage Reference	(Note 3)	VREF	2.5	-	AVDD	V

Notes: 1. All voltages with respect to ground.
2. AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
3. Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=2.83Vpp*VREF/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25℃; AVDD,DVDD=5.0V; VREF=AVDD; fs=44.1kHz; Signal Frequency=1kHz;
$R_L \geqq 10k\Omega$; Measurement Bandwidth=10Hz～20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Dynamic Characteristics (Note 4)					
THD+N		-80	-86		dB
	(Note 5)	-74	-83		
Dynamic Range (A-Weighted)		86	92		dB
	(Note 5)	82	88		
S/N (A-Weighted)		86	92		dB
	(Note 5)	82	88		dB
Interchannel Isolation		80	90		dB
DC Accuracy					
Interchannel Gain Mismatch			0.1	0.2	dB
Gain Drift			60	-	ppm/℃
Analog Output					
Output Voltage	(Note 6)	2.69	2.83	2.97	Vpp
	(Note 5)	1.78	1.87	1.96	Vpp
Load Resistance		10			kΩ
Power Supplies					
Power Supply Current	(Note 7)				
Normal Operation ($\overline{PD}$="H")					
AVDD			12	18	mA
DVDD			6	9	mA
Power-Down-Mode ($\overline{PD}$="L")					
AVDD+DVDD	(Note 8)		10	50	uA
Power Dissipation					
Normal Operation			90	135	mW
Power-Down-Mode	(Note 8)		50	250	uW
Power Supply Rejection			50		dB

Notes:4. Measured by AD725C(SHIBASOKU). Averaging mode.(★)

5. AVDD,DVDD=3.3V

6. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)=2.83Vpp*VREF/5.

7. CLKO pin is open. The typical supply current of DVDD drops to 3mA at 3.3V supply voltage. The AVDD supply current does not change.

8. Power Dissipation in the power-down mode is applied with no external clocks (XTI,BICK,LRCK held "H" or "L").
When using the internal oscillation in the power-down mode, the AK4311 may draw the current of about 3mA.

FILTER CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=3.0～5.5V; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband -0.1dB (Note 9)	PB	0		20.0	kHz
-6.0dB		-	22.05	-	kHz
Stopband (Note 9)	SB	24.1			kHz
Passband Ripple	PR			±0.06	dB
Stopband Attenuation	SA	43			dB
Group Delay (Note 10)	GD	-	14.7	-	1/fs
Digital Filter + Analog Filter					
Frequency Response 0～20.0kHz		-	±0.5	-	dB

Note: 9. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@-0.1dB), SB=0.546*fs(@-43dB).

10. The calculating delay time which occurred by digital filtering. This time is from setting the 16bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=3～5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Input Voltage at AC coupling (XTI pin)	VAC	1	-	-	Vpp
High-Level Output Voltage Iout=-20uA	VOH	DVDD-0.1	-	-	V
Low-Level Output Voltage Iout=20uA	VOL	-	-	0.1	V
Input Leakage Current (Note 11)	Iin	-	-	±10	uA

Note: 11. DEM, TST1 pins have internal pull-down devices, nominally 90kΩ.

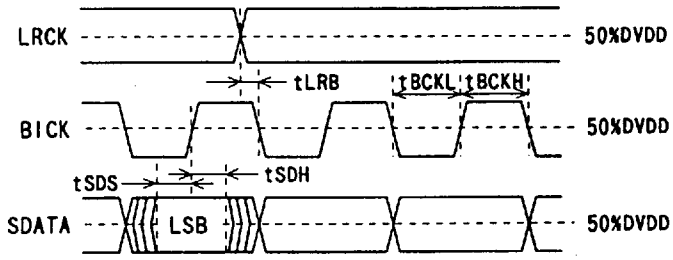
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3~5.5V; C_L=20pF)

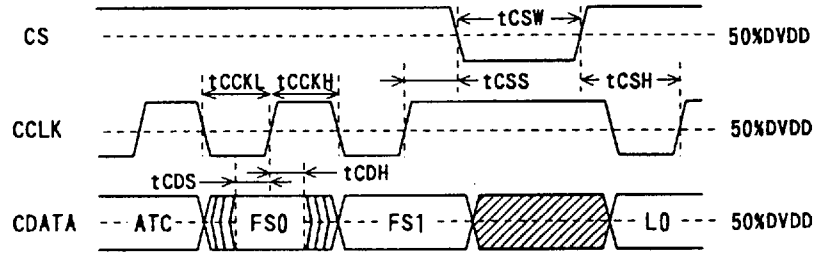
Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency					
Crystal Resonator 256fs:	fCLK	7.1	11.2896	12.8	MHz
384fs:	fCLK	10.7	16.9344	19.2	MHz
External Clock 256fs:	fCLK	2.56	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.84	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Frequency (Note 12)	fs	10	44.1	50	kHz
Audio Interface Timing (Note 13)					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
LRCK Edge to BICK falling (Note 14)	tLRB	-tBCKH+50		tBCKL-50	ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Control Interface Timing (Note 15)					
CCLK Pulse Width Low	tCCKL	100			ns
Pulse Width High	tCCKH	100			ns
CDATA Latch Hold Time	tCDS	50			ns
CDATA Latch Setup Time	tCDH	50			ns
CS Pulse Width Low	tCSW	100			ns
CCLK to CS falling	tCSS	50			ns
CS rising to CCLK	tCSH	50			ns
Reset Timing					
$\overline{PD}$ Pulse Width (Note 16)	tRST	100			ns

Notes: 12. If the duty of LRCK changes lager than ±1/8 from 50%, the AK4311 is reset by the internal phase circuit automatically.
13. Refer to the operating overview section "Audio Data Interface".
14. BICK rising edge must not occur at the same time as LRCK edge.
15. Refer to the operating overview section "Serial Mode Control".
16. The AK4311 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

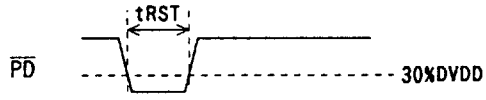
■ Timing Diagram



Audio Data Input Timing



Mode Control Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4311 are XTI(256fs/384fs), LRCK(fs), BICK(32fs~). The master clock (XTI) should be synchronized with LRCK but the phase is free of care. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate(LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). *fs is audio word rate.

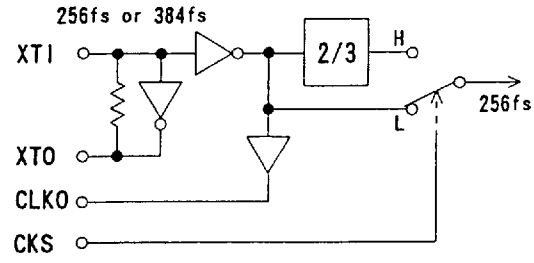


Figure 1. Internal Clock Circuit

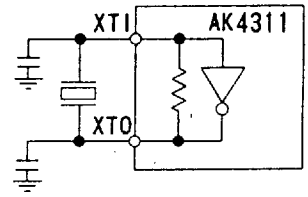


Figure 2. Crystal resonator connection

The master clock can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vpp can be input to the XTI pin by AC coupling. Table 1 illustrates standard audio word rates and corresponding frequencies used in the DAC. When using internal oscillation, CLKO can not be used by external circuit at the power-down mode.

LRCK (fs) (kHz)	CKS	XTI (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

Table 1. Examples of System Clock

As the AK4311 includes the phase detect circuit for LRCK, the AK4311 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not needed except only upon power-up. (Please refer to the "System Reset" section.)

All external clocks(XTI, BICK, LRCK) should always be present whenever the AK4311 is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4311 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4311 should be in the power-down mode($\overline{PD}$="L").

■ Audio Data Interface

The AK4311 has three serial input pins(SDATA, BICK, LRCK). Data bits is clocked into the AK4311 via SDATA pin and is latched by LRCK. The data format is MSB-first, 2's complement and LSB justified.

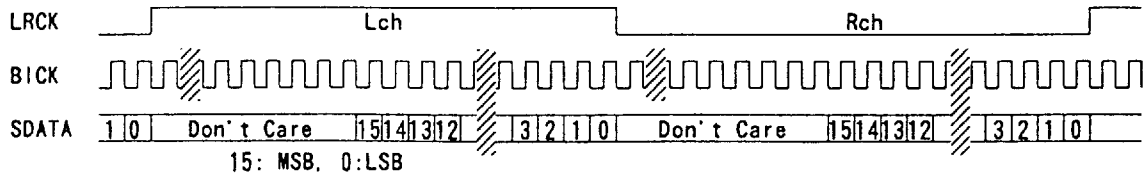


Figure 3. Audio Data Input Format

■ De-emphasis filter

The AK4311 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz, 44.1kHz, 48kHz). De-emphasis is enabled by the following two ways.

1. Way of using DEM pin

Only one de-emphasis(fs=44.1kHz) set initially can be controlled by DEM pin at resetting. The de-emphasis is enabled by setting DEM pin "H". When the frequency of de-emphasis is set by FS0, FS1 of serial mode control bits, the corresponding de-emphasis can be enabled. In this case, DEM bit in the serial mode control should be "0".

2. Way of using serial mode control

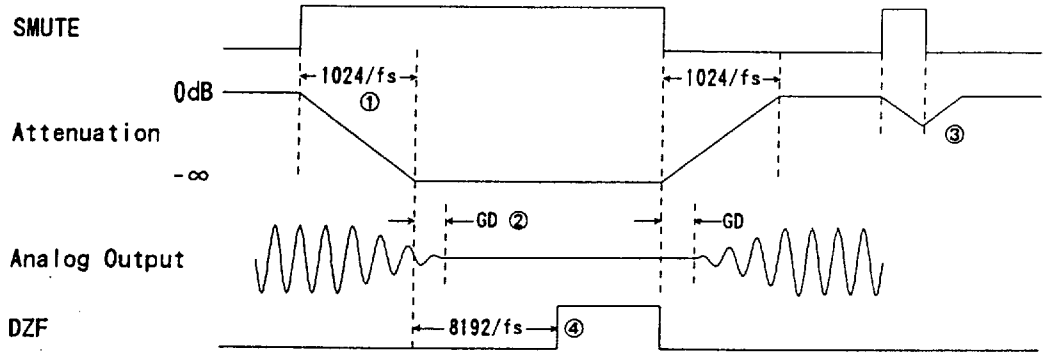
DEM pin should be open or "L". In this case, The de-emphasis corresponding to fs=32kHz, 44.1kHz, 48kHz can be controlled by DEM, FS0 and FS1 in the serial mode control bits.

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmmision.



Notes:

①The output signal is attenuated by -∞ during 1024 LRCK cycles(1024/fs).

②Analog output corresponding to digital input have the group delay(GD).

③If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

Figure 4. Soft mute and zero detection

■ Serial Mode Control

The AK4311 can control output attenuation level, output mode, de-emphasis type and attenuation mode via the serial interface. The serial data consists of two 8 bits for setting the attenuation level of each channel and 8 bits for the mode control.

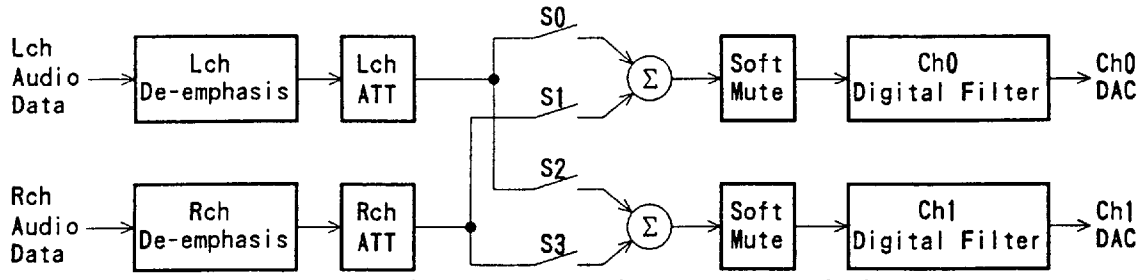
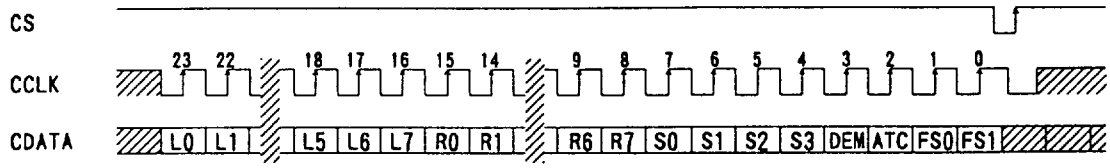


Figure 5. Configuration of attenuator and mixer



L0-L7:	Lch ATT data, L0=LSB, L7=MSB	:FFH at RESET
R0-R7:	Rch ATT data, R0=LSB, R7=MSB	:FFH at RESET
S0-S3:	Output mode Control	:1001 at RESET
DEM:	De-Emphasis Control	:0 at RESET
ATC:	ATT mode Control	:0 at RESET
FS0,FS1:	fs Control for de-emphasis Filter	:00 at RESET

Note: CCLK should be held "H" or "L" except writing to ATT & mode registers in order to avoid the performance degradation.

Figure 6. Serial mode control timing

1. Attenuator Operation

The AK4311 has individually controllable attenuator with linear scale and 256 levels for each channel.

Equation of attenuation level: $ATT = 20 \times Log_{10}(Binary\ level/255)$

FFH: 0dB
|
01H: -48.1dB
00H: Mute (Infinity zero:-∞)

The transition between ATT values is same as soft mute operation. When current value is ATT1 and new value is set as ATT2, ATT1 gradually becomes ATT2 with same operation as soft mute. If new value is set as ATT3 before reaching ATT2, ATT value gradually becomes ATT3 from the way of transition.

Cycle time of soft mute: Ts=1024/fs

When resetting, ATT value is set 00H(Infinity zero). ATT value gradually changes from 00H to FFH(0dB) during Ts after exiting reset.

2. Output mode

The AK4311 supports the following output modes.

- Normal stereo output
- L/R Reverse output
- Monaural mixing output:(L+R)/2
- Output muting with soft mute operation

When resetting, ATT values of both channels are FFH and the attenuation levels are set 0dB. The output mode is also set normal stereo output.

S0	S1	S2	S3	AOUT0	AOUT1	Mode	
0	0	0	0	MUTE	MUTE	MUTE	
0	0	0	1	MUTE	R		
0	0	1	0	MUTE	L		
0	0	1	1	MUTE	(L+R)/2		
0	1	0	0	R	MUTE		
0	1	0	1	R	R		
0	1	1	0	R	L	Reverse	
0	1	1	1	R	(L+R)/2		
1	0	0	0	L	MUTE		
1	0	0	1	L	R	Stereo	* at RESET
1	0	1	0	L	L		
1	0	1	1	L	(L+R)/2		
1	1	0	0	(L+R)/2	MUTE		
1	1	0	1	(L+R)/2	R		
1	1	1	0	(L+R)/2	L		
1	1	1	1	(L+R)/2	(L+R)/2	MONO	

Table 2. Output mode

3. De-emphasis control

DEM bit and DEM pin are ORed internally. The de-emphasis(tc=50/15us) corresponding to fs(sampling frequency) selected by FS0 and FS1 is enabled by setting DEM bit "1" or DEM pin "H". When DEM bit is "0" and DEM pin is "L", the de-emphasis is disabled and the setting of FS0 and FS1 is invalid. The de-emphasis is also disabled at FS0="1" and FS1="0". When resetting, DEM bit is set "0".

For example, when the de-emphasis is controlled by only DEM pin at fs=44.1kHz, DEM, FS0, FS1 bits should be "0". This condition is also set at resetting.

FS0	FS1	Mode
0	0	44.1kHz
1	0	OFF
0	1	48kHz
1	1	32kHz

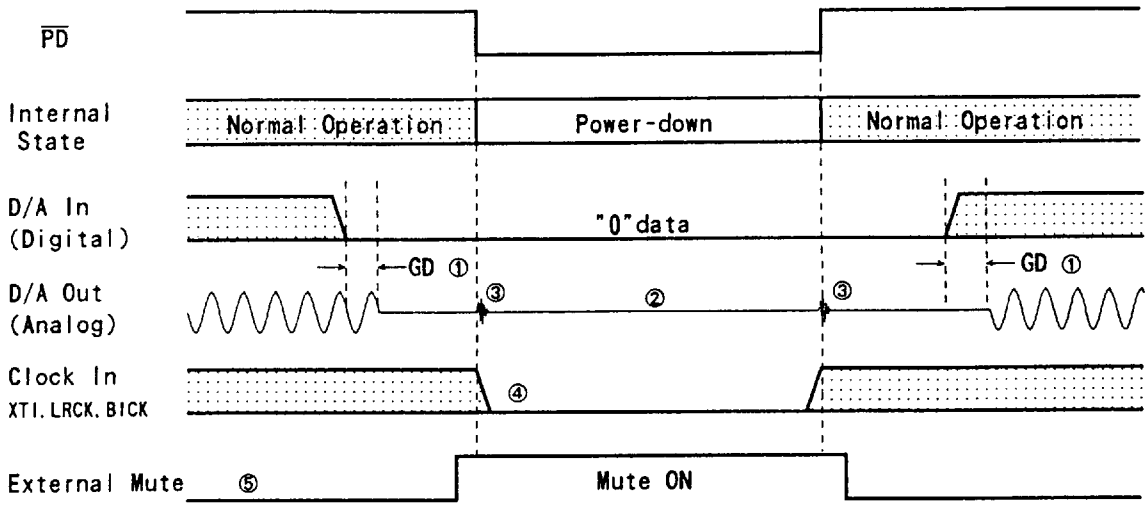
Table 3. De-emphasis filter setting
(Valid at DEM bit="1" or DEM pin="H")

4. Attenuation control

ATT values of both channels are set Lch ATT data by setting ATC bit "1". In this case, Rch ATT data is ignored. When resetting, ATC bit is set "0" (individually control).

■ Power-Down

The AK4311 is placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). ATT value is set 00H at the power-down mode. When exiting the power-down mode, ATT value returns from 00H to FFH(0dB) with soft transition during Ts. Figure 7 shows an example of the system timing at the power-down and power-up.



Notes:

①Analog output corresponding to digital input have the group delay(GD).

②Analog outputs are floating(Hi-Z) at the power-down mode. The output noise level is about -110dB.

③Click noise about -50dB occurs at the edges("↑ ↓") of $\overline{PD}$ signal.

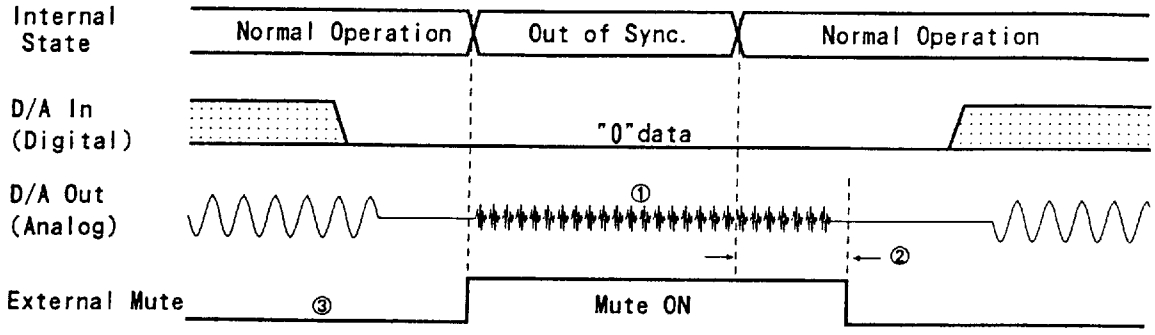
④When the external clocks(XTI, BICK, LRCK) are stopped, the AK4311 should be in the power-down mode.

⑤Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure.

Figure 7. Power-down/up sequence example

■ System Reset

The AK4311 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK "↑" upon exiting reset. If the phase difference between LRCK and internal control signals is larger than +1/16～-1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK. Since RAM address shifts during this synchronization, correct data would not be output until 14 sampled data are input even if the AK4311 returns to the normal operation. Refer to Figure 8.



When cycle ratio between LRCK and XTI can be not kept 1:256(1:384 at 384fs) by changing LRCK frequency etc., internal reset by out-of-synchronization may occur. Some noise occurs at resetting and after returning to normal operation. This noise also occurs even if "0" data is being input to the AK4311.

①Click noise is output continuously when out-of-synchronization occurs continuously.
②Some noise occurs until 14*LRCK cycles after LRCK returns to normal condition.
③Please mute the analog output externally if there is possibility of out of synchronization in the application. The timing example is shown in this figure.

Figure 8. Out-of-synchronization timing example

1. Internal State at resetting by out-of-synchronization(★)

When the AK4311 is reset automatically by out-of-synchronization, the contents of the serial mode control register are kept during out-of-synchronization. Therefore, it is not necessary to resett the serial mode control register. After returning to normal operation, ATT value gradually changes from 00H to the kept value (Figure 9). Some noise occurs at out-of-synchronization and this noise can not be muted perfectly by enabling the SMUTE pin or MUTE bit in the serial mode control register. Please mute the analog outputs by the timing in Figure 8.

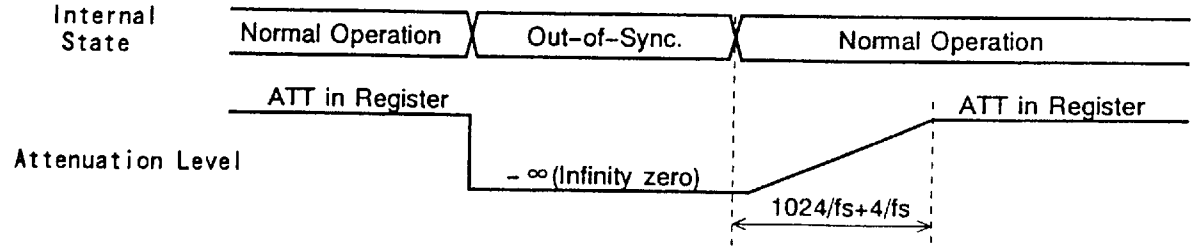


Figure 9. ATT operation at out-of-synchronization

When enabling the SMUTE pin or MUTE bit in the serial mode control register by the timing of Figure 9. The analog output corresponding the input data outputs for an instant because the ATT initial transition and the soft muting operate at the same time. There are 3 ways to avoid this phenomenon.

a. Not use the soft muting. When using the soft muting, the soft muting is disabled before exiting out-of-synchronizationis.
b. Set the input audio data to "0".
c. Set the ATT regiter to 00H.

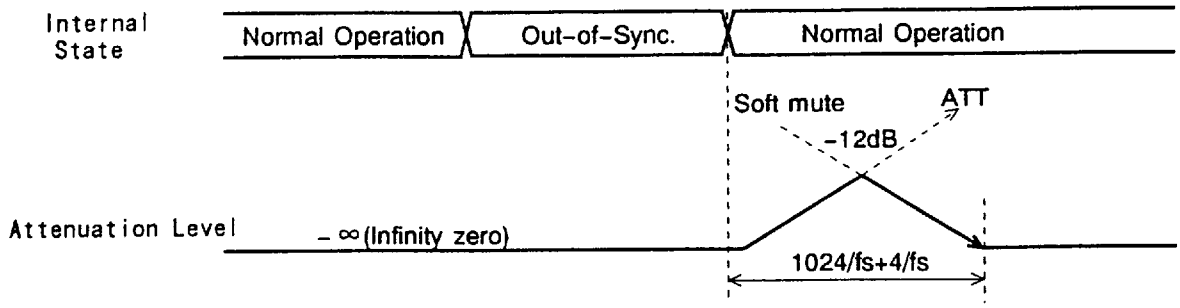


Figure 10. Out-of-synchronization timing with soft muting(@ATT=FFH)
*The solid line shows the actual attenuation level.

2. Cases where out-of-synchronization occurs

- L/R clcok with 2/4 times speed is input to AK4311 in CD-ROM application.
- The clock frequency is not changed smoothly in the PLL system of Satellite Broadcasting application.
- The clock frequency is not changed smoothly between VCO and X'tal in the digital recording application.

SYSTEM DESIGN

Figure 11 shows the system connection diagram. An evaluation board[AKD4311] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

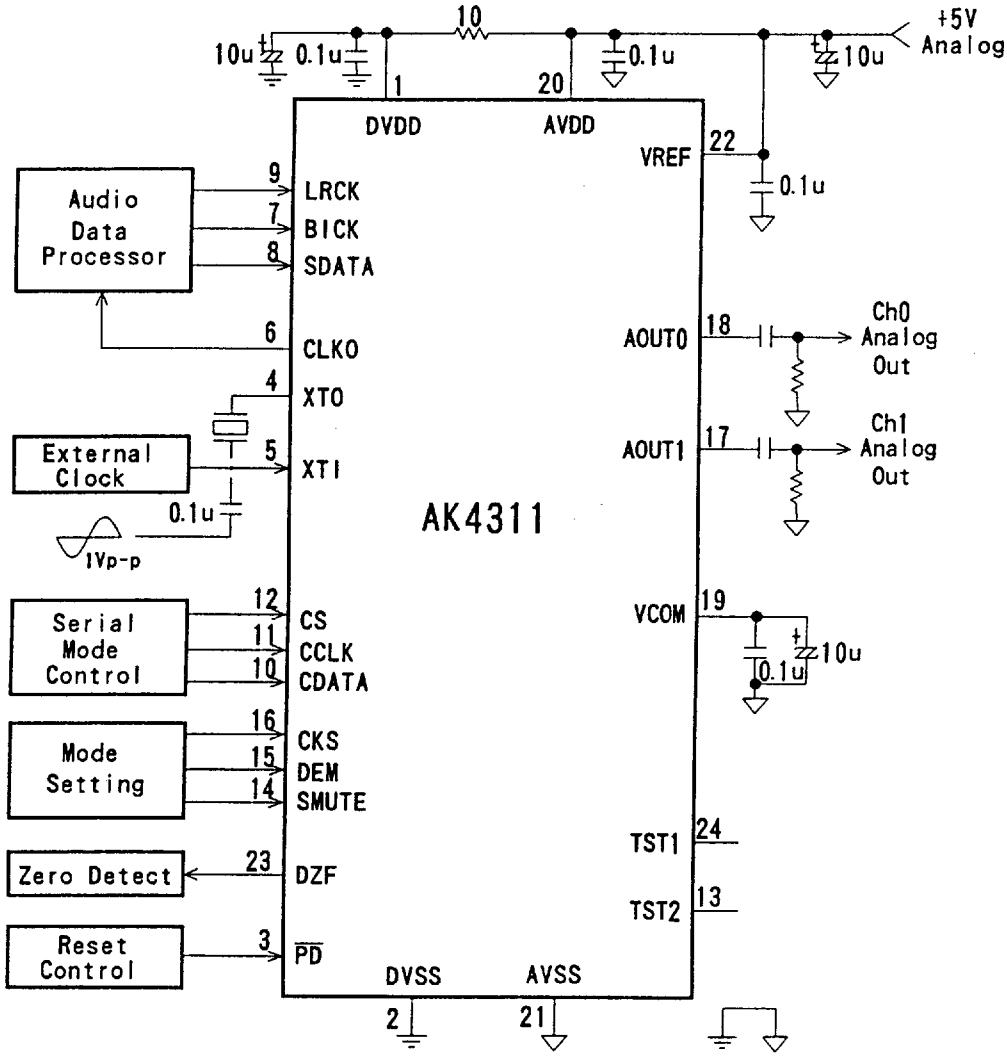


Figure 11. Typical Connection Diagram

Notes:

- LRCK=fs, BICK≧32fs, XTI=256fs at CKS="L", XTI=384fs at CKS="H".
- CCLK should be held "H" or "L" except writing to ATT & mode registers.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be as near to the AK4311 device as possible, with the low value ceramic capacitor of VREF being the nearest.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4311.

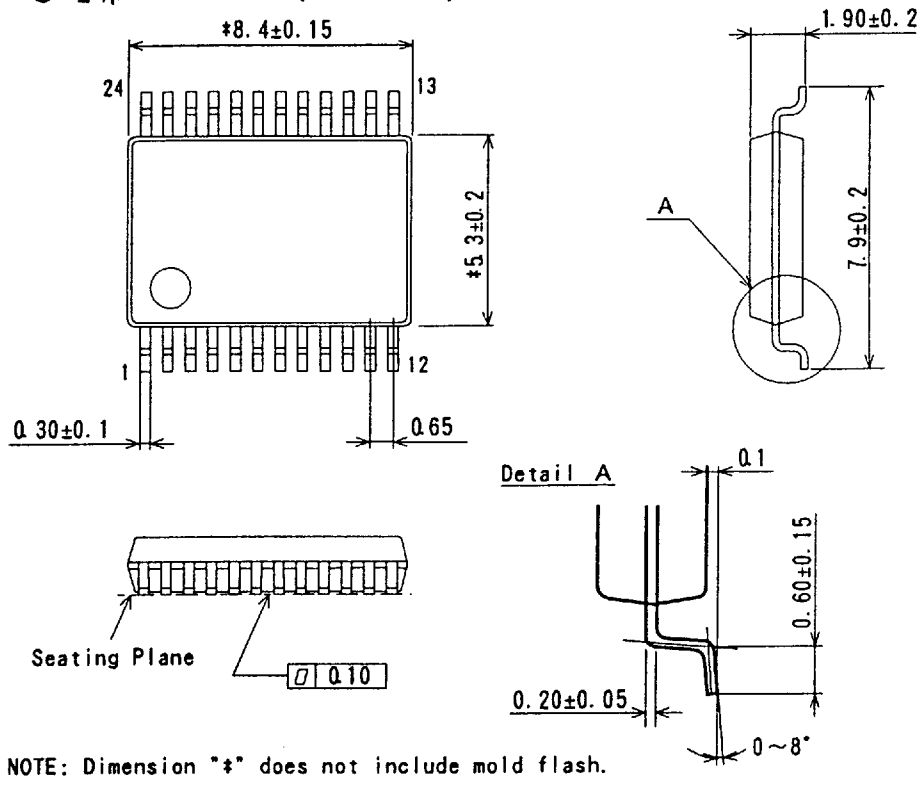
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.83Vpp. AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of a few mV.

PACKAGE

● 24pin SSOP (Unit: mm)

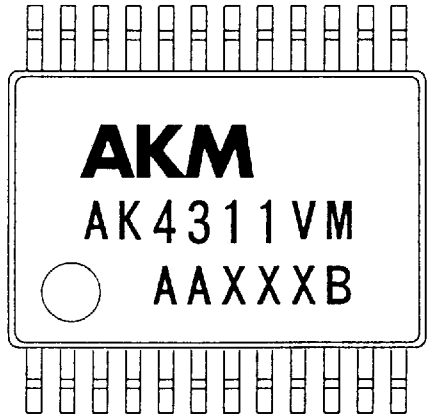


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXB

AA : Lot# (alphabet)

XXXB : Date Code (X : numbers, B : alphabet)