



ES9028PRO

32-Bit HyperStream® II 8-Channel Audio DAC

The **SABRE® ES9028PRO HyperStream® II** 8-channel audio DAC is a high performance 32-bit solution designed for Audiophile and Studio equipment applications such as SACD players, Blu-ray players, digital preamplifier, A/V receivers, studio consoles and digital audio workstations.

| Part Number | Description | Package | DNR (dB) | THD+N (dB) | 32-bit DAC | I ² S / DoP / DSD / SPDIF Input | Jitter Reduction |
|------------------|--|----------|--------------------------|------------|------------|--|------------------|
| ES9028PRO | SABRE® PRO 32-bit 8-ch HyperStream II Audio DAC | 64 eTQFP | 135 (mono) 129 (8-Ch) | –120 | Yes | Yes | Yes |

Using the critically acclaimed ESS' patented **HyperStream® II** architecture and Time Domain Jitter Eliminator, the ES9028PRO 32-Bit Audio DAC delivers an unprecedented DNR of up to 135dB in mono mode and THD+N of –120dB, the industry's highest performance level that will satisfy the needs of the most demanding audio applications.

The **ES9028PRO** handles up to 32-bit 768kHz PCM, DSD256 via DoP and native DSD1024 data in master or slave timing modes. Custom sound signature is supported via a fully programmable FIR filter with 7 presets. Residual distortion from suboptimal PCB components and layout can be minimized using **ES9028PRO's** unique THD compensation circuit, while chip-to-chip gain variation is minimized via a built-in auto gain calibration circuit.

The **SABRE® ES9028PRO** sets the standard for HD audio performance, **SABRE SOUND®**, in a cost-effective, easy-to-use 64-eTQFP package for today's most demanding digital-audio applications.

| FEATURES | BENEFITS |
|---|--|
| Patented 32-bit HyperStream® II DAC <ul style="list-style-type: none"> Up to 135dB DNR (mono mode) –120dB THD+N | <ul style="list-style-type: none"> Industry's highest performance 32-bit audio DAC with unprecedented dynamic range and ultra-low distortion Supports both synchronous and asynchronous sampling modes |
| Patented Time Domain Jitter Eliminator | <ul style="list-style-type: none"> Unmatched audio clarity free from input clock jitter |
| 64-bit accumulator and 32-bit processing | <ul style="list-style-type: none"> Distortion-free signal processing |
| Versatile Digital Input | <ul style="list-style-type: none"> Supports SPDIF, PCM (I²S, LJ, RJ 16-32-bit), DoP or DSD input Supports up to 768kHz PCM, DSD256 via DoP and native DSD1024 Supports up to 1.536MHz external oversampling filter Supports master and slave timing modes |
| Integrated DSP functions | <ul style="list-style-type: none"> Click-free, soft mute and output volume changes Programmable Zero detection De-emphasis for 32kHz, 44.1kHz, and 48kHz sampling |
| Customizable output configuration | <ul style="list-style-type: none"> Mono, stereo, or 8-channel output with either current-mode or voltage-mode operation (current-mode gives lower THD) |
| User Programmable Oversampling Filter | <ul style="list-style-type: none"> 7 ready-to-use preset filters with linear/minimum phase and low-delay options Supports custom coefficients for unique sound signature Supports external oversampling filter |
| Clock Gearing | <ul style="list-style-type: none"> Reduces operating frequency for lower power consumption |
| Gain Calibration ADC | <ul style="list-style-type: none"> Enables uniform output level across all chips |
| THD compensation | <ul style="list-style-type: none"> Minimizes distortion from external PCB components and layout |
| Full 8-to-8 channel mapping | <ul style="list-style-type: none"> Allows channels to be remapped for optimized PCB routing |

APPLICATIONS

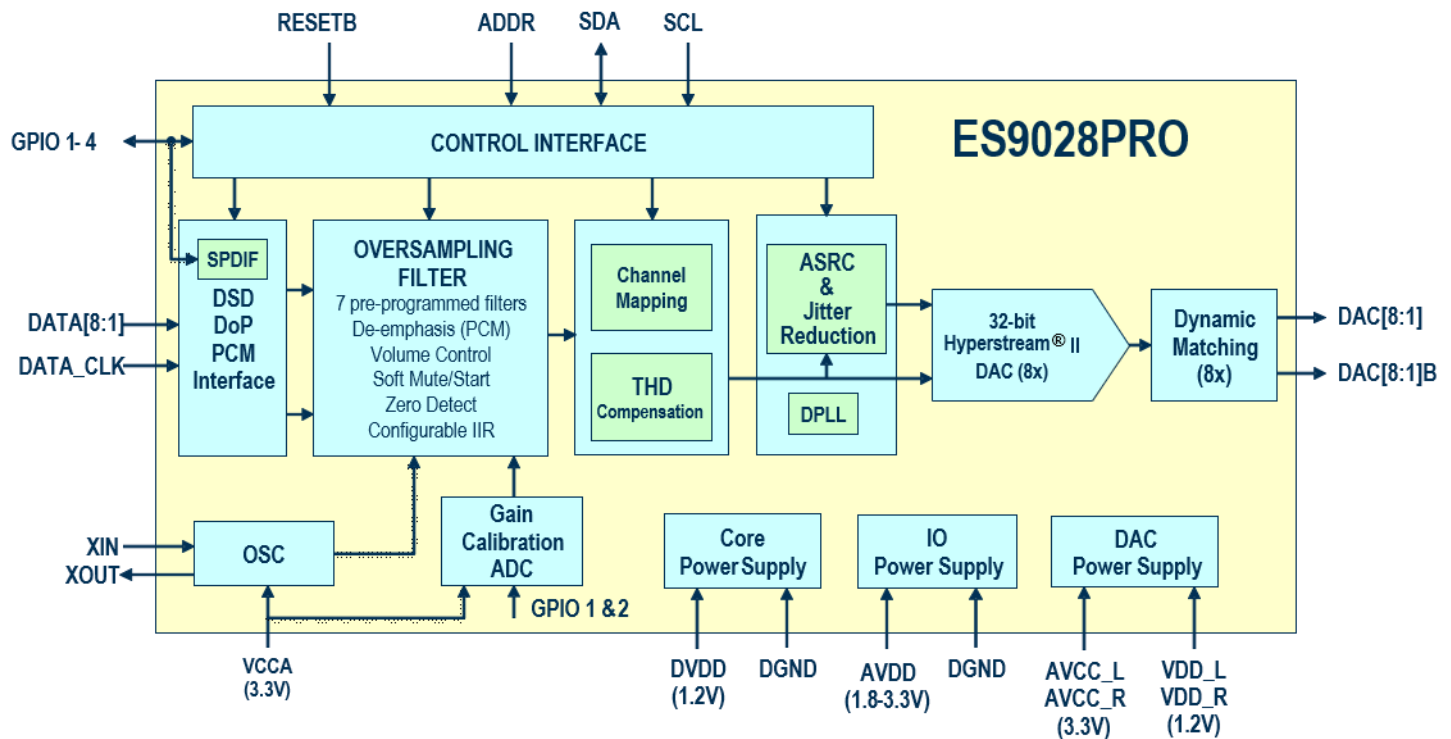
Digital-Audio Workstations
Blu-ray / SACD players

Professional Audio Equipment
A/V Receivers

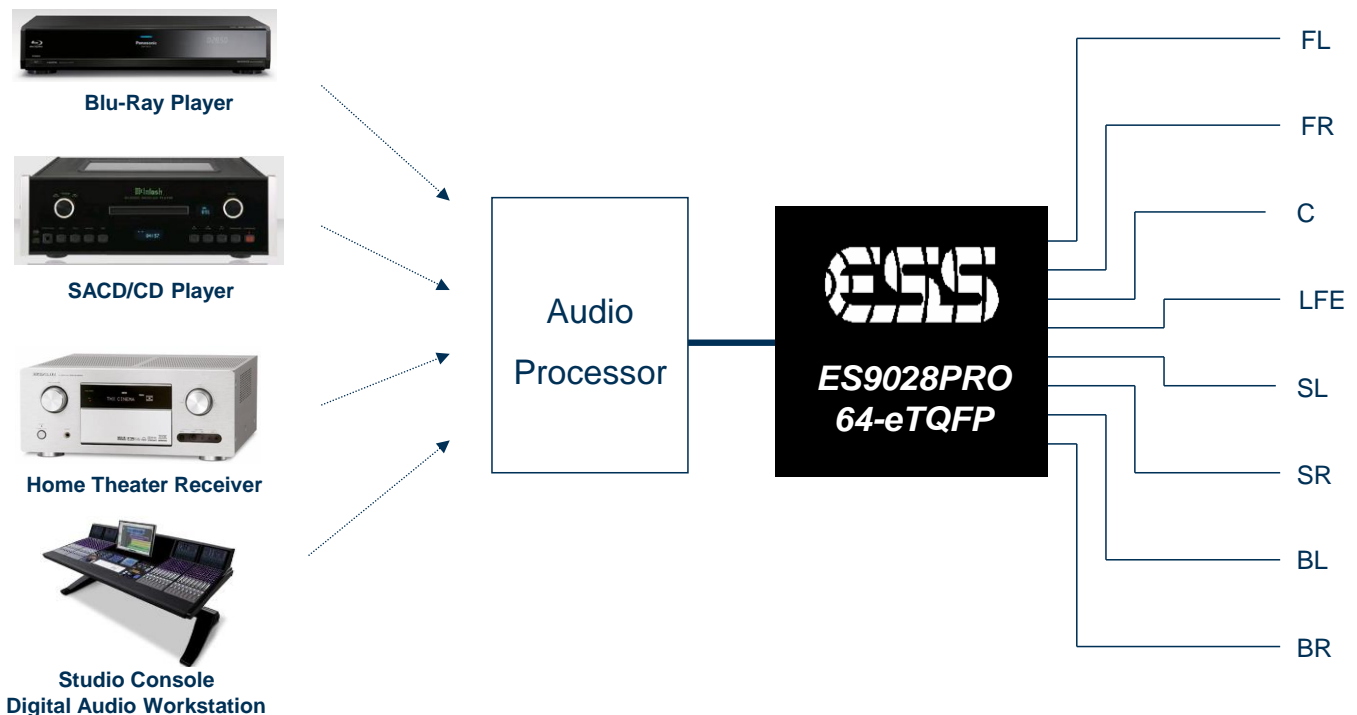


ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

FUNCTIONAL BLOCK DIAGRAM



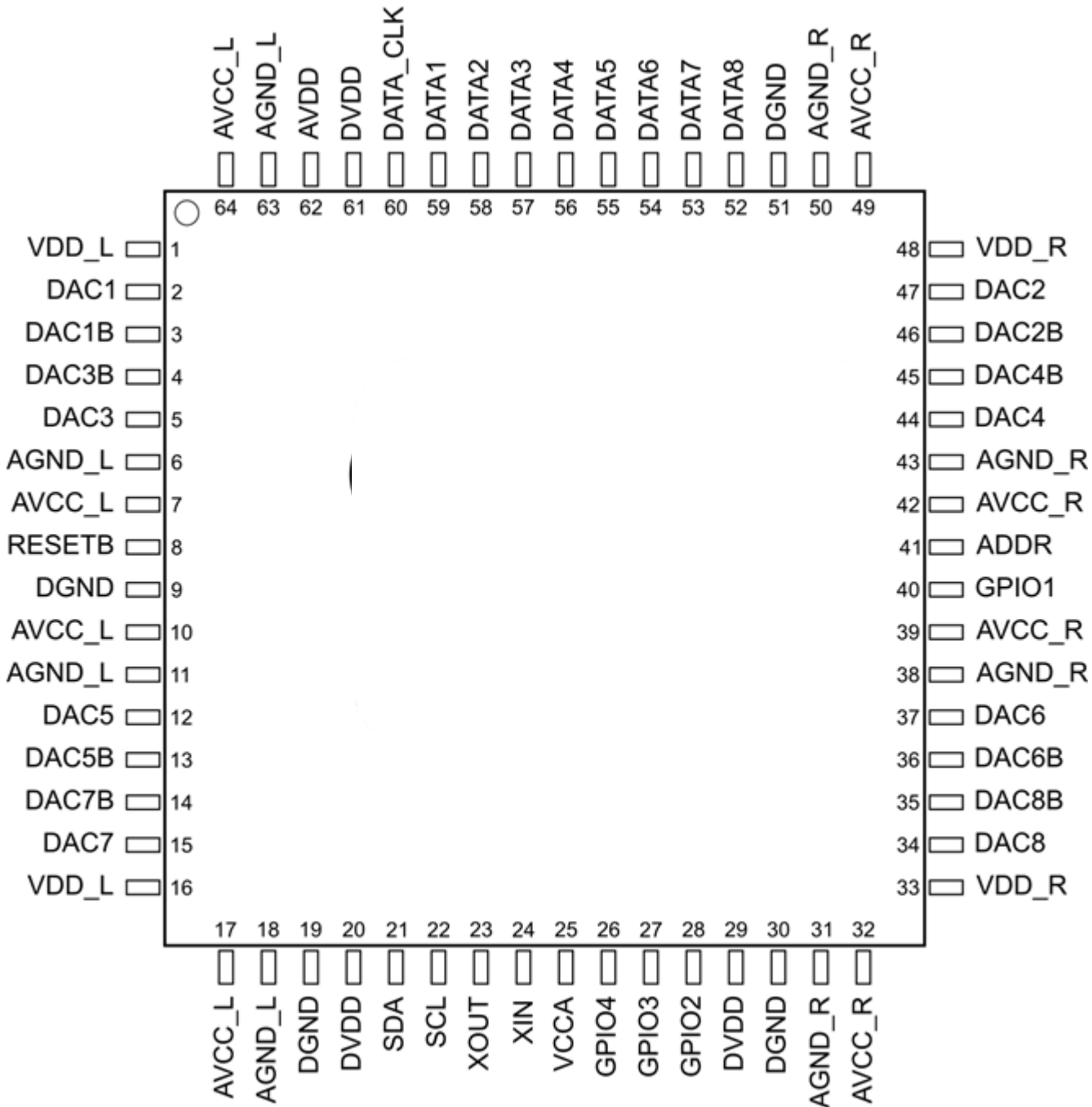
TYPICAL APPLICATION BLOCK DIAGRAM



ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



PIN LAYOUT





ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

PIN DESCRIPTIONS

| Pin | Name | Pin Type | Reset State | Pin Description |
|-----|--------|----------|---------------------------------------|---|
| 1 | VDD_L | Power | Power | Analog Power (+1.2V) for Left channels |
| 2 | DAC1 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 1 |
| 3 | DAC1B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 1 |
| 4 | DAC3B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 3 |
| 5 | DAC3 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 3 |
| 6 | AGND_L | Ground | Ground | Analog Ground for Left channels |
| 7 | AVCC_L | Power | Power | Low-Noise Analog Power (+3.3V) for Left channels |
| 8 | RESETB | I | Tri-stated | Global Reset Input, Active Low |
| 9 | DGND | Ground | Ground | Digital Ground |
| 10 | AVCC_L | Power | Power | Low-Noise Analog Power (+3.3V) for Left channels |
| 11 | AGND_L | Ground | Ground | Analog Ground for Left channels |
| 12 | DAC5 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 5 |
| 13 | DAC5B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 5 |
| 14 | DAC7B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 7 |
| 15 | DAC7 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 7 |
| 16 | VDD_L | Power | Power | Analog Power (+1.2V) for Left channels |
| 17 | AVCC_L | Power | Power | Low-Noise Analog Power (+3.3V) for Left channels |
| 18 | AGND_L | Ground | Ground | Analog Ground for Left channels |
| 19 | DGND | Ground | Ground | Digital Ground |
| 20 | DVDD | Power | Power | Digital Power (+1.2V) for core logic |
| 21 | SDA | I/O | Tri-stated | I ² C Serial Data Input / Output |
| 22 | SCL | I | Tri-stated | I ² C Serial Clock Input |
| 23 | XOUT | AO | Floating | Crystal oscillator output |
| 24 | XIN | AI | Floating | Crystal oscillator input (Note: can also just be a clock input) |
| 25 | VCCA | Power | Power | Power (+3.3V) for oscillator / Gain Calibration |
| 26 | GPIO4 | I/O | Tri-stated | GPIO 4 |
| 27 | GPIO3 | I/O | Tri-stated | GPIO 3 |
| 28 | GPIO2 | I/O | Tri-stated | GPIO 2 |
| 29 | DVDD | Power | Power | Digital Power (+1.2V) for core of chip |
| 30 | DGND | Ground | Ground | Digital Ground |
| 31 | AGND_R | Ground | Ground | Analog Ground for Right channels |
| 32 | AVCC_R | Power | Power | Low-Noise Analog Power (+3.3V) for Right channels |
| 33 | VDD_R | Power | Power | Analog Power (+1.2V) for Right channels |
| 34 | DAC8 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 8 |
| 35 | DAC8B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 8 |
| 36 | DAC6B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 6 |
| 37 | DAC6 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 6 |
| 38 | AGND_R | Ground | Ground | Analog Ground for Right channels |
| 39 | AVCC_R | Power | Power | Low-Noise Analog Power (+3.3V) for Right channels |

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PIN DESCRIPTIONS (continued)

| Pin | Name | Pin Type | Reset State | Pin Description |
|-------------|----------|----------|---------------------------------------|---|
| 40 | GPIO1 | I/O | Tri-stated | GPIO 1 |
| 41 | ADDR | I | Tri-stated | Chip Address Select |
| 42 | AVCC_R | Power | Power | Low-Noise Analog Power (+3.3V) for Right channels |
| 43 | AGND_R | Ground | Ground | Analog Ground for Right channels |
| 44 | DAC4 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 4 |
| 45 | DAC4B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 4 |
| 46 | DAC2B | AO | Driven to ground via R _{DAC} | Differential Negative Analog Output 2 |
| 47 | DAC2 | AO | Driven to ground via R _{DAC} | Differential Positive Analog Output 2 |
| 48 | VDD_R | Power | Power | Analog Power (+1.2V) for Right channels |
| 49 | AVCC_R | Power | Power | Low-Noise Analog Power (+3.3V) for Right channels |
| 50 | AGND_R | Ground | Ground | Analog Ground for Right channels |
| 51 | DGND | Ground | Ground | Digital Ground |
| 52 | DATA8 | I/O | Tri-stated | DSD Data8 or SPDIF Input 9 |
| 53 | DATA7 | I/O | Tri-stated | DSD Data7 or SPDIF Input 8 |
| 54 | DATA6 | I/O | Tri-stated | DSD Data6 or SPDIF Input 7 |
| 55 | DATA5 | I/O | Tri-stated | DSD Data5 or PCM Data CH7 / CH8 or SPDIF Input 6 |
| 56 | DATA4 | I/O | Tri-stated | DSD Data4 or PCM Data CH5 / CH6 or SPDIF Input 5 |
| 57 | DATA3 | I/O | Tri-stated | DSD Data3 or PCM Data CH3 / CH4 or SPDIF Input 4 |
| 58 | DATA2 | I/O | Tri-stated | DSD Data2 or PCM Data CH1 / CH2 or SPDIF Input 3 |
| 59 | DATA1 | I/O | Tri-stated | DSD Data1 or PCM Frame Clock or SPDIF Input 2 |
| 60 | DATA_CLK | I/O | Tri-stated | PCM Bit Clock or DSD Bit Clock or SPDIF Input 1 |
| 61 | DVDD | Power | Power | Digital Power (+1.2V) for core of chip |
| 62 | AVDD | Power | Power | Digital Power (+1.8V / +3.3V) for top pad ring of chip |
| 63 | AGND_L | Ground | Ground | Analog Ground for Left channels |
| 64 | AVCC_L | Power | Power | Low-Noise Analog Power (+3.3V) for Left channels |
| Exposed Pad | | | | Can be left open, connected to digital or analog ground. Internally connected to substrate via a conductive epoxy |

Notes:

VDD_L, VDD_R and DVDD are internally connected.

I = Digital Input I/O = Input / Output

AI = Analog Input AO = Analog Output

All unused digital inputs should be connected to ground directly, or via a pull-down resistor of 4.7kΩ to 47kΩ

5V Tolerant Pins (3.3V AVDD Supply Only)

The following pins are 5V tolerant:

- RESETB
- SDA and SCL
- GPIO1-4
- ADDR
- DATA1-8
- DATA_CLK



System Clock and Audio Inputs

Sampling Rate Notations

| Mode | FSR raw sample rate at audio interface | fs sample rate for filter specification |
|------------------------------|--|---|
| DSD | DATA_CLK | FSR / 64 |
| DoP | Frame Clock Rate | FSR / 4 |
| Serial (PCM) Normal Mode | Frame Clock Rate | FSR |
| Serial (PCM) OSF Bypass Mode | Frame Clock Rate | FSR / 8 |
| SPDIF | SPDIF Audio Rate | FSR |

System Clock (XIN) and Audio Master Clock (MCLK)

The system clock (XIN) can be generated with a crystal using the built-in oscillator or supplied externally.

- The maximum XIN frequency is 100MHz as specified in [ANALOG PERFORMANCE](#) and [XIN Timing](#).
- The audio master clock (MCLK) is divided down from XIN via *clock_gear* in [Register 0: System Registers](#).
- The minimum MCLK frequency for a given raw sample rate FSR is specified in [ANALOG PERFORMANCE](#).
- The minimum MCLK frequency for a given I2C clock is specified in the table under [I2C Timing Table](#).

PCM Pin Connections

| Pin Name | Description |
|----------|--------------------------------|
| DATA1 | Frame clock |
| DATA5~2 | 8-channel PCM serial data |
| DATA_CLK | Bit clock for PCM audio format |

Note: DATA_CLK frequency must be $(2 \times \text{serial_length}) \times \text{FSR}$.

serial_length can be set in [Register 2: Serial Data Configuration and Automute Enable](#)

SPDIF Pin Connections

| Pin Name | Description |
|----------|-------------------|
| GPIO4~1 | SPDIF input 13~10 |
| DATA8~1 | SPDIF input 9~2 |
| DATA_CLK | SPDIF input 1 |

An SPDIF source multiplexer allows for up to 13 SPDIF sources to be connected to the data and GPIO pins selectable via [Register 11: SPDIF Mux and GPIO Inversion](#). SPDIF input mode can be manually selected by *input_select* in [Register 1: Input selection](#) or automatically selected if *auto_select* in [Register 1: Input selection](#) is set to a mode allowing automatic SPDIF selection.

DSD Pin Connections

| Pin Name | Description |
|----------|------------------------------|
| DATA8~1 | 8-channel DSD data input |
| DATA_CLK | Bit clock for DSD data input |

Note: DATA_CLK frequency must be FSR.

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Master Mode

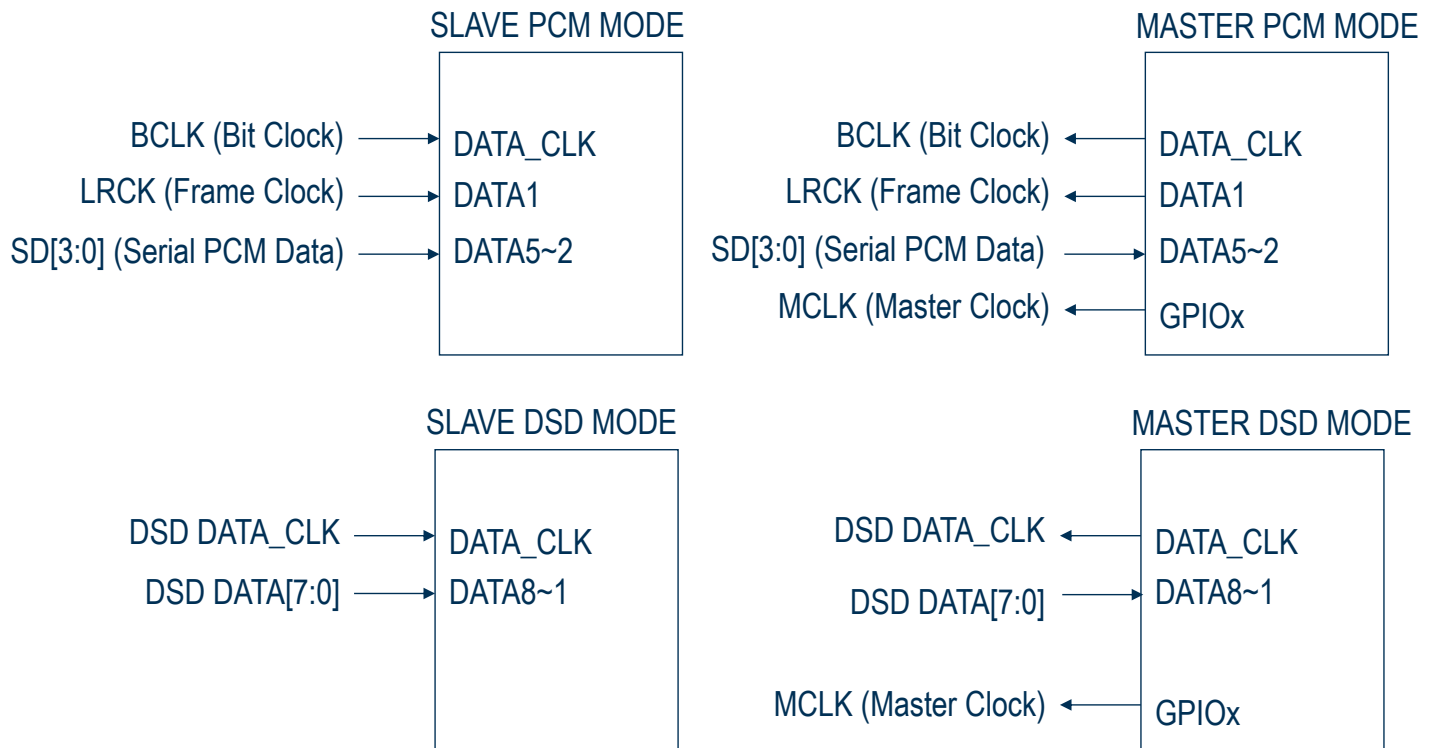
The DAC can become an audio timing master via *master_mode* in [Register 10: Master Mode and Sync Configuration](#).

- The 'input_select' bits in [Register 1: Input selection](#) must be set correctly to select either DSD or serial master mode.

The Bit Clock frequency can be configured using one of the following two methods:

- Set the desired *master_div* in [Register 10: Master Mode and Sync Configuration](#), or
- Use NCO mode to set FSR using [Register 42-45: Programmable NCO](#). When in NCO mode the *master_div* setting will be ignored.

An available GPIO pin can be configured to output MCLK using [Register 8: GPIO1-2 Configuration](#) and [Register 9: GPIO3-4 Configuration](#).





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Function Description

Soft Mute

When Mute is asserted the output signal will ramp to the $-\infty$ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is set by [Register 6: De-emphasis Filter & Volume Ramp Rate](#) according to the following relationship:

$$\text{rate} = \frac{2^{\text{vol_rate}} * \text{FSR}}{512} \text{ dB/s}$$

Automute (PCM and SPDIF modes only)

Automute is disabled by default and can be enabled by setting *automute_time* to a non-zero value. Automute is triggered when the following conditions are met:

| Mode | Detection Condition | Time |
|--------------|---|--|
| PCM SPDIF | Data is lower than <i>automute_level</i> for the specified time | $\frac{2096896}{\text{automute_time} * \text{FSR}} \text{ (s)}$ |

Automute_time can be set using [Register 4: Automute Time](#).

Automute_level can be set using [Register 5: Automute Level](#).

The automute status can be read using *automute_status* in [Register 64: Chip ID and Status](#) or via a GPIO pin programmed as *Automute Status* using [Register 8: GPIO1-2 Configuration](#) or [Register 9: GPIO3-4 Configuration](#).

The triggered automute behavior can be configured using [Register 2: Serial Data Configuration and Automute Enable](#) to one of the followings:

- No action
- Soft Mute
- Ramp all channels to ground to reduce power consumption
- Soft Mute then ramp all channels to ground

The ramp-to-ground rate can be configured to $4096 * \frac{2^{(\text{soft_start_time}+1)}}{\text{MCLK}}$ using [Register 14: Soft-Start Configuration](#).

Volume Control

Each channel has an independently controlled digital attenuation circuit which can be set to attenuate from 0dB to -127dB in 0.5dB steps. When a new volume level is set, the digital attenuation circuit will ramp softly to the new level. To ensure silent digital volume transitions each 0.5dB step can take as many as 64 intermediate steps depending on the *volume_rate* setting in [Register 6: De-emphasis Filter & Volume Ramp Rate](#).

Master Trim

The master trim sets the 0dB reference level for the digital volume control of each DAC. The master trim is programmable via [Register 24-27: Master Trim](#). The master trim registers store a 32bit signed number and should never exceed the full scale signed value 32'h7FFFFFFF.

18dB Channel Gain (PCM mode only)

A +18dB gain can be applied on a per-channel based using [Register 62: +18dB Channel Gain](#), in addition to volume control and master trim. Note that the output will be clipped if the +18dB gain results in larger than full scale output.

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De-emphasis

The de-emphasis feature is included for audio data that has utilized the 50/15µs pre-emphasis for noise reduction. There are three de-emphasis filters, one for 32kHz, one for 44.1kHz, and one for 48kHz selectable via *deemph_sel* and bypassed via *deemph_bypass* in [Register 6: De-emphasis Filter & Volume Ramp Rate](#).

The de-emphasis filter can automatically be applied when an SPDIF stream sets the de-emphasis flag. It will auto detect the sample rate (32k, 44.1k, 48k) in either consumer or professional formats and then apply the correct de-emphasis filter. The automatic enabling of the de-emphasis filter can be enabled via *auto_deemph* in [Register 6: De-emphasis Filter & Volume Ramp Rate](#).

Preset Oversampling FIR Filters

Seven pre-programmed digital filters are selectable for SPDIF and PCM serial mode via *filter_shape* in [Register 7: Filter Bandwidth and System Mute](#). See [ANALOG PERFORMANCE](#), [PCM FILTER FREQUENCY RESPONSE](#) and [PCM FILTER IMPULSE RESPONSE](#) for more information.

Custom Oversampling FIR Filter

The FIR filter can also be programmed as a two-staged interpolation filter with custom coefficients to achieve unique sound signature. Custom coefficients can be generated using MATLAB and then downloaded using a custom C code.

Example Source Code for Loading a Filter

```
// only accept 128, 64 or 16 coefficients
// Note: The coefficients must be quantized to 32 bits for this method!
// Note: Stage 1 consists of 128 or 64 values (0-127 being the coefficients)
// Note: Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note: Stage 2 is symmetric about coefficient 13. See the example filters for more information.
byte fir_badr = 32;
byte coeff_stage = (byte)(coeffs.Count == 64 ? 0 : 1);
for (int i = 0; i < coeffs.Count; i++)
{
    // stage 1 contains 128 or 64 coefficients, while stage 2 contains 16 coefficients
    registers.WriteRegister(fir_badr, (byte)((coeff_stage << 7) + i));

    // write the coefficient data
    registers.WriteRegister(fir_badr+1, (byte)(coeffs[i] & 0xff));
    registers.WriteRegister(fir_badr+2, (byte)((coeffs[i] >> 8) & 0xff));
    registers.WriteRegister(fir_badr+3, (byte)((coeffs[i] >> 16) & 0xff));

    registers.WriteRegister(fir_badr+5, 0x02); // set the write enable bit
}
// disable the write enable bit when we're done
registers.WriteRegister(fir_badr+5, (byte)(setEvenBit ? 0x04 : 0x00));
```

Oversampling Filter (OSF) Bypass

The oversampling FIR filter can be bypassed using *bypass_osf* in [Register 37: Programmable FIR Configuration](#), sourcing data directly into the IIR filter. The audio input should be oversampled at 8 x fs rate when OSF is bypassed to have the same IIR filter bandwidth as PCM audio sampled at fs rate. For example, a signal with 44.1kHz sample rate can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I²S, LJ, or RJ format. The maximum sample rate that can be applied is 1.536MHz (8 x 192kHz).

IIR Filter

Four filters with cutoffs at 47kHz, 50kHz, 60kHz, and 70kHz scaled by fs/44100 are selectable via *iir_bw* in [Register 7: Filter Bandwidth and System Mute](#). See [ANALOG PERFORMANCE](#) and [IIR FILTER RESPONSE](#) for more information.



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Time Domain Jitter Eliminator and DPLL

By default, the DAC works in Jitter Eliminator mode allowing the audio interface timing to be asynchronous to MCLK. A DPLL constantly updates the FSR/MCLK ratio to calculate the true 32-bit timing of the incoming audio samples allowing the ESS patented Time Domain Jitter Eliminator to remove any distortion caused by jitter.

- The DPLL acquisition speed can be set by *lock_speed* in [Register 10: Master Mode and Sync Configuration](#).
- The PCM/SPDIF DPLL bandwidth can be set via *dppl_bw_serial* in [Register 12: Jitter Eliminator / DPLL Bandwidth](#)
- The DSD DPLL bandwidth can be set via *dppl_bw_dsd* in [Register 12: Jitter Eliminator / DPLL Bandwidth](#)

For best performance, the DPLL bandwidth should be set to the minimum setting that will keep the DPLL reliably in lock.

Sample Rate Calculation

The raw sample rate (FSR) can be calculated from [Register 66-69 : DPLL Number](#) using the following formula:

$$FSR = \frac{(dppl_num * MCLK)}{2^{32}}$$

Synchronous Mode (PCM mode only)

The DPLL can be bypassed if the incoming PCM audio is synchronous to MCLK with the relationship $MCLK=128FSR$. This can be enabled via *128fs_mode* in [Register 10: Master Mode and Sync Configuration](#).

DAC Full-Scale Gain Calibration

DAC gain calibration enables uniform output level across multiple chips by compensating for chip-to-chip gain variations.

The DAC full-scale gain-calibration system works by comparing an internal resistor to an external precision resistor of known value. The two resistors are set up as a voltage divider that is connected between power and ground. The value of the internal resistor changes with semiconductor process variations so by measuring the divider's voltage output, using an ADC, the process variation from nominal can be measured and this is used to correct the DAC gain. As all the DAC channels are on the same monolithic chip, the channel-to-channel gain variation is very small and does not need to be trimmed.

There are two ADCs and either of the ADC inputs can be used to drive the auto-calibration circuit. The circuit uses the ADC value, as decimated by the internal programmable decimation filters, to scale the *master_trim* value. *Master_trim* can be programmed as normal but will be scaled by the ADC value when in automatic-calibration mode. In this mode, *master_trim* can be set once by enabling automatic calibration, and the DAC output levels will be consistent across all DAC devices.

- Full-scale gain-calibration is enabled using *calib_en* in [Register 63: Auto Calibration](#).
- *calib_sel* in [Register 63: Auto Calibration](#) selects which ADC to use
- *calib_latch* in [Register 63: Auto Calibration](#) determines whether to use the new ADC correction value or ignore it.
- ADC values update at the *ADC_CLK* rate which is also programmable in [Register 46: ADC Configuration](#).

The ADC decimation filters may also be programmed to a lower bandwidth to help smooth out any voltage transients on the divider output.

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THD Compensation

THD Compensation can be used to minimize distortion from external PCB components and layout through the generation of inverse second and third harmonic components matching the target system distortion profile.

THD compensation can be enabled via *thd_enb* in [Register 13: Jitter Eliminator / DPLL Configuration & THD Bypass](#). The coefficient for manipulating second harmonic distortion is stored in [Register 28-29: THD Compensation C2](#). The coefficient for manipulating third harmonic distortion is stored in [Register 30-31: THD Compensation C3](#).

All channels use the same compensation coefficients.

Full Channel Mapping, Mono Mode and Stereo Mode

Channel mapping allows output channels to be remapped to arbitrary input channels for optimized PCB routing

Clearing *stereo_mode* in [Register 15: GPIO Input Selection & Volume Configuration](#) allows the data for each DAC to be sourced from any input channel using [Registers 38-41: DAC Channel Mapping](#).

- Mono mode can be implemented by channel mapping all output DAC sources to the same input channel

Setting *stereo_mode* in [Register 15: GPIO Input Selection & Volume Configuration](#) will source DAC channels 1/3/5/7 and channels 2/4/6/8 from input channel 1 and 2.

In SPDIF mode, DAC channels 1/3/5/7 and channels 2/4/6/8 are sourced from SPDIF input left and right channels.

Power Supplies

To minimize THD+N, AVCC_L and AVCC_R must be powered by low-noise +3.3V supplies. Although AVCC_L and AVCC_R could be powered from a single low-noise supply, crosstalk would be compromised and so separate +3.3V supplies are highly recommended. The ES9311Q dual ultra-low noise regulator is designed to power AVCC_L and AVCC_R and minimize THD+N and crosstalk on all SABRE PRO DACs.

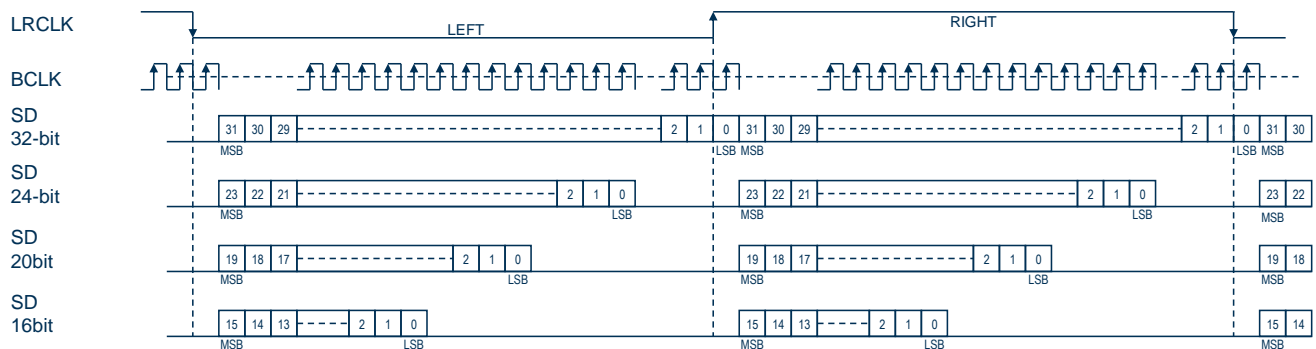
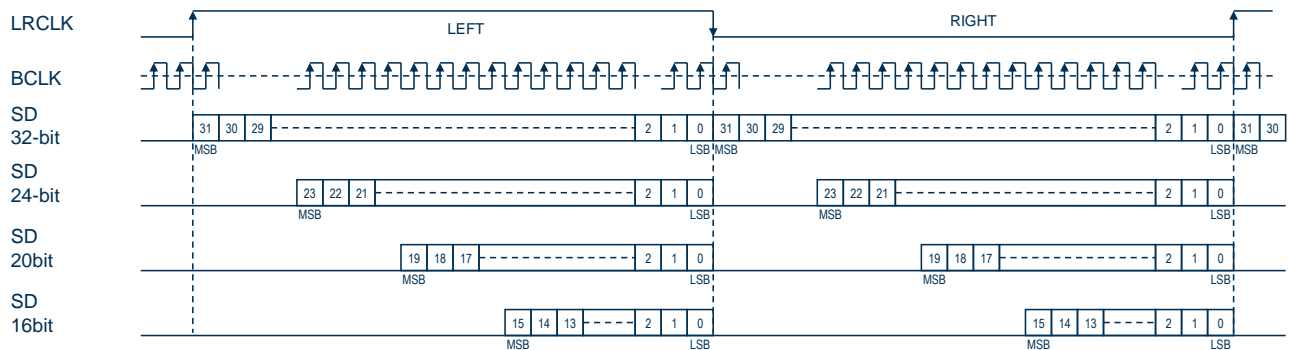
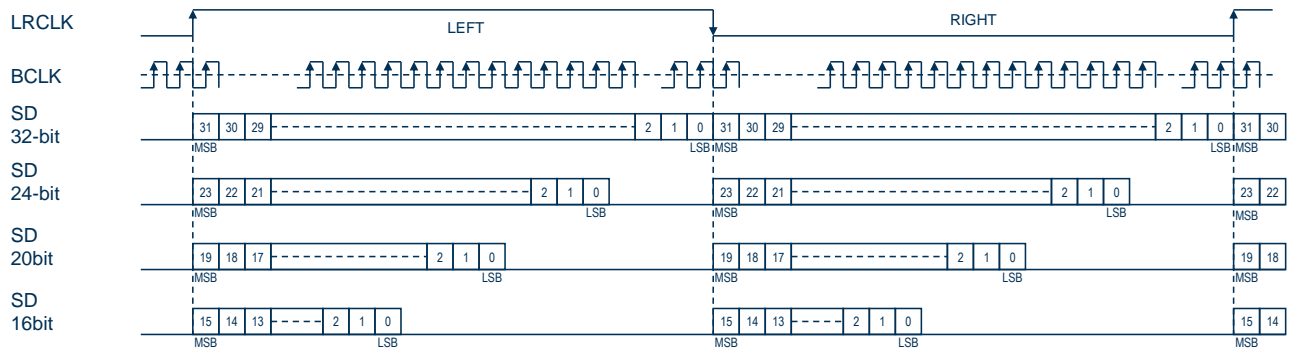


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Audio Interface Formats

Several digital audio transport formats are supported to allow direct connection to common audio processors. Auto detection circuitry is enabled by default to detect the input format. The input mode can be explicitly set using [Register 1: Input selection](#). The following diagrams outline the supported formats (using stereo 2-channel inputs as an example).

PCM LJ, RJ and I2S Formats



The following number of BCLK edges are present per frame (left plus right):

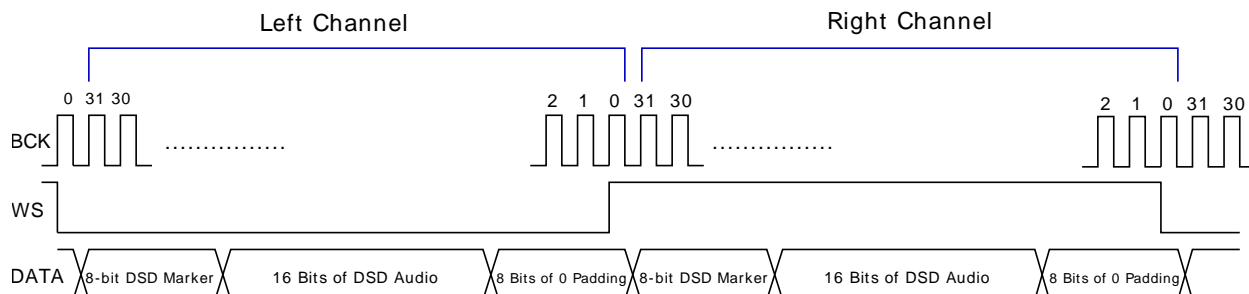
- 16-bit mode: 32 BCLKs
- 24-bit mode: 48 BCLKs
- 32-bit mode: 64 BCLKs

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DoP (DSD over PCM) Audio Format

The DoP format packs DSD data into PCM frames. The incoming data is identified as DoP if the DSD Markers 0x05 and 0xFA alternating each frame clock cycle are present as illustrated below.

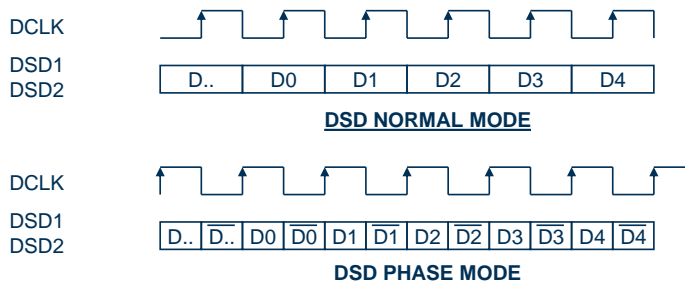


| Frame Cycle | 1 Left | 1 Right | 2 Left | 2 Right | 3 Left | 3 Right |
|-------------|--------|---------|--------|---------|--------|---------|
| DSD Marker | 0x05 | 0x05 | 0xFA | 0xFA | 0x05 | 0x05 |

Note: DoP requires 24-bit or 32-bit PCM mode and cannot be handled by 16-bit PCM mode.

- 24-bit mode: DoP data consists of 8-bit marker in the MSB followed by 16-bit DSD data
- 32-bit mode: DoP data consists of 8-bit marker in the MSB followed by 16-bit DSD data and 8-bit padding

Native DSD Format

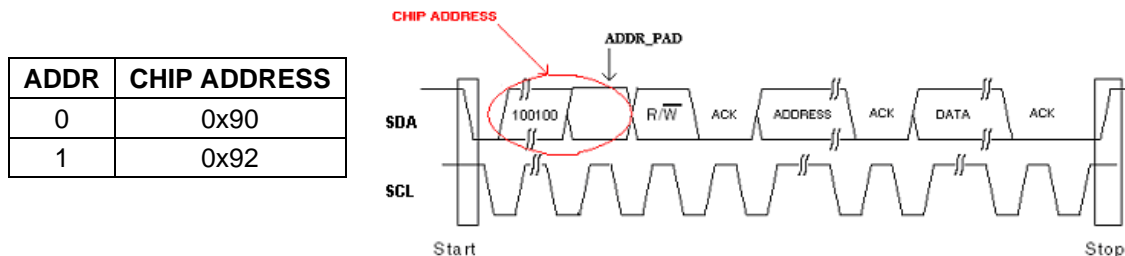




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Serial Control Interface

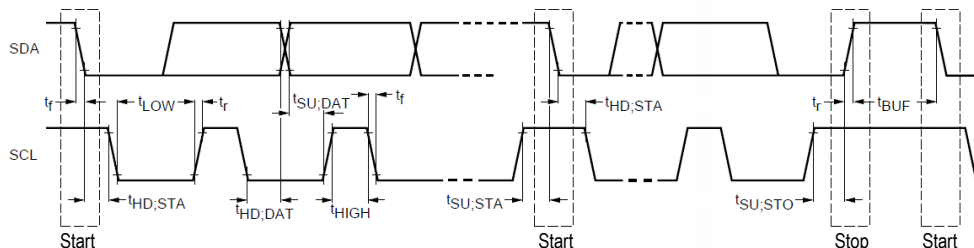
The registers inside the chip are programmed via an I²C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings via the “ADDR” pin.



Notes:

1. The “ADDR” pin is used to create the CHIP ADDRESS. (0x90, 0x92)
2. The first byte after the CHIP ADDRESS (“ADDRESS”) is the register address.
3. The second byte after the CHIP ADDRESS (“DATA”) is the data to be programmed into the register.
4. Multi-byte reads are NOT supported and will cause the I²C decoder to become unresponsive until a reset occurs.

I²C Timing Table



| Parameter | Symbol | MCLK Constraint | Standard-Mode | | Fast-Mode | | Unit |
|-------------------------------------|---------------------|-----------------|---------------|------|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| SCL Clock Frequency | f _{SCL} | < MCLK/20 | 0 | 100 | 0 | 400 | kHz |
| START condition hold time | t _{HD,STA} | | 4.0 | - | 0.6 | - | μs |
| LOW period of SCL | t _{LOW} | >10/MCLK | 4.7 | - | 1.3 | - | μs |
| HIGH period of SCL (>10/MCLK) | t _{HIGH} | >10/MCLK | 4.0 | - | 0.6 | - | μs |
| START condition setup time (repeat) | t _{SU,STA} | | 4.7 | - | 0.6 | - | μs |
| SDA hold time from SCL falling | t _{HD,DAT} | | 0 | - | 0 | - | μs |
| SDA setup time from SCL rising | t _{SU,DAT} | | 250 | - | 100 | - | ns |
| Rise time of SDA and SCL | t _r | | - | 1000 | | 300 | ns |
| Fall time of SDA and SCL | t _f | | - | 300 | | 300 | ns |
| STOP condition setup time | t _{SU,STO} | | 4 | - | 0.6 | - | μs |
| Bus free time between transmissions | t _{BUF} | | 4.7 | - | 1.3 | - | μs |
| Capacitive load for each bus line | C _b | | - | 400 | - | 400 | pF |

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REGISTER SETTINGS

Note: Multi-byte registers use little-endian byte ordering scheme with the least significant byte stored at the lowest register address and most significant byte stored at the highest register address.

Register 0: System Registers

| Bits | [7:4] | [3:2] | [1] | [0] |
|----------|---------|----------|----------|------------|
| Mnemonic | osc_drv | clk_gear | reserved | soft_reset |
| Default | 4'b0000 | 2'b00 | 1'b0 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|------------|---|
| [7:4] | osc_drv | <p>Oscillator drive specifies the bias current to the oscillator pad.</p> <ul style="list-style-type: none"> 4'b1111: shut down the oscillator 4'b1110: 1/4 bias 4'b1100: 1/2 bias 4'b1000: 3/4 bias 4'b0000: full bias (default) |
| [3:2] | clk_gear | <p>Configures a clock divider network that can reduce the power consumption of the chip by reducing the clock frequency supplied to both the digital core and analog stages.</p> <ul style="list-style-type: none"> 2'b00: MCLK = XIN (default) 2'b01: MCLK = XIN / 2 2'b10: MCLK = XIN / 4 2'b11: MCLK = XIN / 8 |
| [1] | reserved | |
| [0] | soft_reset | <p>Software configurable hardware reset with the ability to reset the design to its initial power-on configuration.</p> <ul style="list-style-type: none"> 1'b1: resets the SABRE DAC to its power-on defaults 1'b0: normal operation (default) <p>Note: This register will always read as "1'b0" as the power-on default for this register is "1'b0". A reset can be verified by checking the status of other modified registers.</p> |



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Register 1: Input selection

| Bits | [7] | [6] | [5] | [4] | [3:2] | [1:0] |
|----------|-----------|---------------|----------------|----------|-------------|--------------|
| Mnemonic | user_bits | spdif_ig_data | spdif_ig_valid | reserved | auto_select | input_select |
| Default | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 2'b11 | 2'b00 |

| Bit | Mnemonic | Description |
|-------|----------------|--|
| [7] | user_bits | Both SPDIF channel status bits and SPDIF user bits are available for readback via the I2C interface. To reduce register count, the channel status bits and user bits occupy the same register space. Setting user_bits will present the SPDIF user bits on the read-only register interface instead of the default channel status bits. <ul style="list-style-type: none"> 1'b1: presents the SPDIF user bits on the read-only register interface 1'b0: presents the SPDIF channel status bits on the read-only register interface (default) |
| [6] | spdif_ig_data | Configures the SPDIF decoder to ignore the 'data' flag in the channel status bits. <ul style="list-style-type: none"> 1'b1: ignore the data flag in the channel status bits and continue to process the decoded SPDIF data 1'b0: mute the SPDIF data when the data flag is set (default) Note: Enabling the SPDIF output when data is present could cause undesirable noise if the SPDIF data is compressed audio or a non-standard format. |
| [5] | spdif_ig_valid | Configures the SPDIF decoder to ignore the 'valid' flag in the SPDIF stream. <ul style="list-style-type: none"> 1'b1: ignore the valid flag and continue to process the decoded SPDIF data 1'b0: mute the SPDIF data when the valid flag is invalid (default) |
| [4] | reserved | |
| [3:2] | auto_select | Allows the SABRE DAC to automatically select between either serial, SPDIF or DSD input formats. <ul style="list-style-type: none"> 2'b11: automatically select between DSD, SPDIF or serial data (default) 2'b10: automatically select between SPDIF or serial data 2'b01: automatically select between DSD or serial data 2'b00: disable automatic input decoder and instead use the information provided by register 1[1:0] |
| [1:0] | input_select | Configures the SABRE DAC to use a particular input decoder if auto_select is disabled. <ul style="list-style-type: none"> 2'b11: DSD 2'b10: reserved 2'b01: SPDIF 2'b00: serial (default) Note: Register 1[3:2] must be set to 2'b00 for input_select to function. |

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Register 2: Serial Data Configuration and Automute Enable

| Bits | [7:6] | [5:4] | [3:2] | [1:0] |
|----------|-----------------|-------------|---------------|-------------|
| Mnemonic | automute_config | serial_bits | serial_length | serial_mode |
| Default | 2'b00 | 2'b11 | 2'b11 | 2'b00 |

| Bit | Mnemonic | Description |
|-------|-----------------|---|
| [7:6] | automute_config | <p>Configures the automute state machine, which allows the SABRE DAC to perform different power saving and sound optimizations.</p> <ul style="list-style-type: none"> 2'b11: perform a mute and then ramp all channels to ground when an automute condition is asserted 2'b10: ramp all channels to ground when an automute condition is asserted 2'b01: perform a mute when an automute condition is asserted 2'b00: normal operation (default) <p>Note: Ramping DAC outputs to ground can reduce the power consumption of the SABRE DAC in some situations.</p> <p>Note: This process can be sped up by using the <i>automute_time</i>, <i>volume_rate</i> and <i>soft_start_time</i> registers.</p> |
| [5:4] | serial_bits | <p>Selects how many bits consist of a data word in the serial data stream.</p> <ul style="list-style-type: none"> 2'b11: 32-bit data words (default) 2'b10: 32-bit data words 2'b01: 24-bit data words 2'b00: 16-bit data words |
| [3:2] | serial_length | <p>Selects how many DATA_CLK pulses exist per data word.</p> <ul style="list-style-type: none"> 2'b11: 32-bit data words (default) 2'b10: 32-bit data words 2'b01: 24-bit data words 2'b00: 16-bit data words |
| [1:0] | serial_mode | <p>Configures the type of serial data.</p> <ul style="list-style-type: none"> 2'b11 or 2'b10: right-justified mode 2'b01: left-justified mode 2'b00: I2S mode (default) |



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Register 3: Reserved

| | |
|----------|-------------|
| Bits | [7:0] |
| Mnemonic | reserved |
| Default | 8'b00000000 |

Register 4: Automute Time

| | |
|----------|---------------|
| Bits | [7:0] |
| Mnemonic | automute_time |
| Default | 8'd0 |

| Bit | Mnemonic | Description |
|-------|---------------|---|
| [7:0] | automute_time | <p>Configures the amount of time the audio data must remain below the <i>automute_level</i> before an automute condition is flagged. Defaults to 0 which disables automute.</p> $\text{Time in seconds} = \frac{2096896}{\text{automute_time} * \text{FSR}}$ |

Register 5: Automute Level

| | | |
|----------|----------|----------------|
| Bits | [7] | [6:0] |
| Mnemonic | reserved | automute_level |
| Default | 1'b0 | 7'd104 |

| Bit | Mnemonic | Description |
|-------|----------------|---|
| [7] | reserved | |
| [6:0] | automute_level | <p>Configures the threshold which the audio must be below before an automute condition is flagged. The level is measured in decibels (dB) and defaults to -104dB.</p> <p>Note: This register works in tandem with <i>automute_time</i> to create the automute condition.</p> |

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Register 6: De-emphasis Filter & Volume Ramp Rate

| Bits | [7] | [6] | [5:4] | [3] | [2:0] |
|----------|-------------|---------------|------------|----------|-------------|
| Mnemonic | auto_deemph | deemph_bypass | deemph_sel | reserved | volume_rate |
| Default | 1'b0 | 1'b1 | 2'b00 | 1'b1 | 2'b010 |

| Bit | Mnemonic | Description |
|-------|---------------|---|
| [7] | auto_deemph | <p>Automatically engages the de-emphasis filters when SPDIF data is provides and the SPDIF channel status bits contains valid de-emphasis settings.</p> <ul style="list-style-type: none"> 1'b1: enables automatic de-emphasis 1'b0: disables automatic de-emphasis (default) |
| [6] | deemph_bypass | <p>Enables or disables the built-in de-emphasis filters.</p> <ul style="list-style-type: none"> 1'b1 disabled de-emphasis filters (default) 1'b0 enables de-emphasis filters |
| [5:4] | deemph_sel | <p>Selects which de-emphasis filter is used.</p> <ul style="list-style-type: none"> 2'b11: reserved 2'b10: 48kHz 2'b01: 44.1kHz 2'b00: 32kHz (default) |
| [3] | reserved | Must be set to 1'b1 (default) for normal operation |
| [2:0] | volume_rate | <p>Selects a volume ramp rate to use when transitioning between different volume levels. The volume ramp rate is measured in decibels per second (dB/s). Volume rate is in the range 0-7.</p> $\text{rate} = \frac{2^{\text{vol_rate}} * \text{FSR}}{512} \text{ dB/s}$ |



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Register 7: Filter Bandwidth and System Mute

| Bits | [7:5] | [4:3] | [2:1] | [0] |
|----------|--------------|----------|--------|------|
| Mnemonic | filter_shape | reserved | iir_bw | mute |
| Default | 3'b010 | 2'b00 | 2'b00 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|--------------|---|
| [7:5] | filter_shape | <p>Selects the type of filter to use during the 8x FIR interpolation phase.</p> <ul style="list-style-type: none"> 3'b111: brickwall filter 3'b110: hybrid, fast roll-off, minimum phase filter 3'b100: apodizing, fast roll-off, linear phase filter 3'b101: reserved 3'b011: slow roll-off, minimum phase filter 3'b010: fast roll-off, minimum phase filter (default) 3'b001: slow roll-off, linear phase filter 3'b000: fast roll-off, linear phase filter <p>Note: The FIR filter is only applied to PCM data, DSD bypasses this phase</p> |
| [4:3] | reserved | |
| [2:1] | iir_bw | <p>Selects the type of filter to use during the 8x IIR interpolation phase.</p> <ul style="list-style-type: none"> 2'b11: 1.5873fs (70k @ 44.1kHz) 2'b10: 1.3605fs (60k @ 44.1kHz) 2'b01: 1.1338fs (50k @ 44.1kHz) 2'b00: 1.0757fs (47.44k @ 44.1kHz) (default) <p>Note: 47.44k filter should only be used for PCM data. Recommended settings for DSD data are 50k, 60k or 70k.</p> |
| [0] | mute | <p>Mutes all 8 channels of the SABRE DAC.</p> <ul style="list-style-type: none"> 1'b1: mute all eight channels 1'b0: normal operation (default) |

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Register 8: GPIO1-2 Configuration

| | | |
|----------|-----------|-----------|
| Bits | [7:4] | [3:0] |
| Mnemonic | gpio2_cfg | gpio1_cfg |
| Default | 4'd8 | 4'd8 |

Register 9: GPIO3-4 Configuration

| | | |
|----------|-----------|-----------|
| Bits | [7:4] | [3:0] |
| Mnemonic | gpio4_cfg | gpio3_cfg |
| Default | 4'd8 | 4'd8 |

GPIO Table

The GPIO can each be configured in one of several ways.
The table below is for programming each independent GPIO configuration value.

| gpioX_cfg | Name | I/O Direction | Details |
|-----------|-------------------------|---------------|--|
| 4'd 0 | Automute Status | Output | Output is high when an automute has been triggered. This signal is analogous to the automute_status register (register 64). |
| 4'd 1 | Lock Status | Output | Output is high when lock is triggered. This signal is analogous to the lock_status register (register 64). |
| 4'd 2 | Volume Min | Output | Output is high when all digital volume controls have been ramped to minus full scale. This can occur, for example, if automute is enabled and set to mute the volume. |
| 4'd 3 | CLK | Output | Output is a buffered MCLK signal which can be used to synchronize other devices. |
| 4'd 4 | Automute/Lock Interrupt | Output | Output is high when the contents of register 64 have been modified (meaning that the lock_status or automute_status register have been changed). Reading register 64 will clear this interrupt. |
| 4'd 5 | ADC_CLK | Output | Output is a buffered ADC clock signal. The ADC clock signal is defined by the adc_clk_sel register. |
| 4'd 6 | Reserved | | |
| 4'd 7 | Output 1'b0 | Output | Output is forced low |
| 4'd 8 | Standard Input | Input | Places the GPIO into a high impedance state, allowing the customer to provide a digital signal and then read that signal back via the I2C register 65. |
| 4'd 9 | Input Select | Input | Places the GPIO into a high impedance state and allows the customer to toggle the input selection between two modes using the GPIO. See register 15 for more information. |
| 4'd 10 | Mute All | Input | Places the GPIO into a high impedance state and allows the customer to force a mute condition by applying a logic high signal to the GPIO. When a logic low signal is applied the DAC will exhibit normal operation. |
| 4'd 11 | Reserved | | |
| 4'd 12 | Reserved | | |



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| | | | |
|--------|--|--------|--|
| 4'd 13 | gpio1_cfg and gpio2_cfg <ul style="list-style-type: none"> ADC Input gpio3_cfg and gpio4_cfg Reserved | Input | <ul style="list-style-type: none"> gpio1_cfg: GPIO1 becomes ADC2 input gpio2_cfg: GPIO2 becomes ADC1 input |
| 4'd 14 | Soft Start Complete | Output | Output is high when the DAC output is ramped to ground. The DAC can be ramped to ground via an automute condition when appropriately programmed, or via register 14. |
| 4'd 15 | Output 1'b1 | Output | Output is forced high |

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Register 10: Master Mode and Sync Configuration

| Bits | [7] | [6:5] | [4] | [3:0] |
|----------|-------------|------------|------------|------------|
| Mnemonic | master_mode | master_div | 128fs_mode | lock_speed |
| Default | 1'b0 | 2'b00 | 1'b0 | 4'd0 |

| Bit | Mnemonic | Description |
|-------|-------------|---|
| [7] | master_mode | <p>Enables master mode which causes the SABRE DAC to derive the DATA_CLK and DATA1 signals when in I2S mode. Can also be enabled when in DSD mode to enable DATA_CLK only.</p> <ul style="list-style-type: none"> 1'b1: enables master mode 1'b0: disables master mode (default) |
| [6:5] | master_div | <p>Sets the frame clock (DATA1) and DATA_CLK frequencies when in master mode. This register is used when in normal synchronous operation.</p> <ul style="list-style-type: none"> 2'b00: DATA_CLK frequency = MCLK/2 (default) 2'b01: DATA_CLK frequency = MCLK/4 2'b10: DATA_CLK frequency = MCLK/8 2'b11: DATA_CLK frequency = MCLK/16 |
| [4] | 128fs_mode | <p>Enables operation of the DAC while in synchronous mode with a 128*FSR MCLK in PCM normal or OSF bypass mode only.</p> <ul style="list-style-type: none"> 1'b1: enables MCLK = 128*FSR mode 1'b0: disables MCLK = 128*FSR mode (default) |
| [3:0] | lock_speed | <p>Sets the number of audio samples required before the DPLL and jitter eliminator lock to the incoming signal. More audio samples give a better initial estimate of the MCLK/FSR ratio at the expense of a longer locking interval.</p> <ul style="list-style-type: none"> 4'd0: 16384 FSL edges (default) 4'd1: 8192 FSL edges 4'd2: 5461 FSL edges 4'd3: 4096 FSL edges 4'd4: 3276 FSL edges 4'd5: 2730 FSL edges 4'd6: 2340 FSL edges 4'd7: 2048 FSL edges 4'd8: 1820 FSL edges 4'd9: 1638 FSL edges 4'd10: 1489 FSL edges 4'd11: 1365 FSL edges 4'd12: 1260 FSL edges 4'd13: 1170 FSL edges 4'd14: 1092 FSL edges 4'd15: 1024 FSL edges <p>Note: FSL=FSR except in DSD Mode FSL=FSR*64</p> |



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Register 11: SPDIF Mux and GPIO Inversion

| | | |
|----------|-----------|-------------|
| Bits | [7:4] | [3:0] |
| Mnemonic | spdif_sel | invert_gpio |
| Default | 4'd0 | 4'b0000 |

| Bit | Mnemonic | Description |
|-------|-------------|--|
| [7:4] | spdif_sel | <p>Selects which input to use when decoding SPDIF data. Note: If using a GPIO the GPIO configuration must be set to an input.</p> <ul style="list-style-type: none"> 4'd0: DATA_CLK (default) 4'd1: DATA1 4'd2: DATA2 4'd3: DATA3 4'd4: DATA4 4'd5: DATA5 4'd6: DATA6 4'd7: DATA7 4'd8: DATA8 4'd9: GPIO1 4'd10: GPIO2 4'd11: GPIO3 4'd12: GPIO4 4'd13-4'd15: Reserved |
| [3:0] | invert_gpio | <p>Inverts each of the GPIO outputs when set. For example, to invert GPIO1 set invert_gpio[0] to 1'b1. GPIOs are non-inverted by default.</p> |

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Register 12: Jitter Eliminator / DPLL Bandwidth

| | | |
|----------|----------------|-------------|
| Bits | [7:4] | [3:0] |
| Mnemonic | dp1l_bw_serial | dp1l_bw_dsd |
| Default | 4'd5 | 4'd10 |

| Bit | Mnemonic | Description |
|-------|----------------|--|
| [7:4] | dp1l_bw_serial | <p>Sets the bandwidth of the DPLL when operating in I2S/SPDIF mode.</p> <ul style="list-style-type: none"> 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: (default) 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth |
| [3:0] | dp1l_bw_dsd | <p>Sets the bandwidth of the DPLL when operating in DSD mode.</p> <ul style="list-style-type: none"> 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: (default) 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth |



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Register 13: Jitter Eliminator / DPLL Configuration & THD Bypass

| Bits | [7] | [6] | [5] | [4:0] |
|----------|---------------|---------|---------------|----------|
| Mnemonic | ns_dither_enb | thd_enb | jitterelim_en | reserved |
| Default | 1'b0 | 1'b0 | 1'b1 | 4'd0 |

| Bit | Mnemonic | Description |
|-------|---------------|---|
| [7] | ns_dither_enb | <p>Selects whether to enable dither in the noise shaped modulators. Dither is enabled by default and helps with maintaining the best possible performance of the modulators.</p> <ul style="list-style-type: none"> 1'b0: enable dither (default) 1'b1: disable dither |
| [6] | thd_enb | <p>Selects whether to disable the THD compensation logic. THD compensation is enabled by default and can be configured to correct for second and third harmonic distortion.</p> <ul style="list-style-type: none"> 1'b0: enable THD compensation (default) 1'b1: disable THD compensation |
| [5] | jitterelim_en | <p>Enables the jitter eliminator and DPLL circuitry.</p> <ul style="list-style-type: none"> 1'b0: disable jitter eliminator 1'b1: enable jitter eliminator (default) |
| [4:0] | reserved | |

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Register 14: Soft-Start Configuration

| Bits | [7] | [6] | [5] | [4:0] |
|----------|------------|---------------------|----------|-----------------|
| Mnemonic | soft_start | soft_stop_on_unlock | reserved | soft_start_time |
| Default | 1'b1 | 1'b0 | 1'b0 | 5'd10 |

| Bit | Mnemonic | Description |
|-------|---------------------|---|
| [7] | soft_start | <p>The Sabre DAC initializes both DAC and DACB to GND, and then ramps up the signal to AVCC/2. DAC and DACB remain in phase until the ramp is complete. <i>Soft_start</i> controls the ramp operation and defaults to 1'b1 (ramp to AVCC/2)</p> <ul style="list-style-type: none"> 1'b0: ramps the output stream to ground 1'b1: normal operation (default) will ramp the output stream to AVCC/2 |
| [6] | soft_stop_on_unlock | <p>Automatically ramps the output low when lock is lost</p> <ul style="list-style-type: none"> 1'b0: do not force the output low on loss of lock (default) 1'b1: force output to ground on loss of lock |
| [5] | reserved | |
| [4:0] | Soft_start_time | <p>Sets the amount of time it takes to perform a soft-start ramp. This time affects ramp to ground & ramp to AVCC/2. The value is valid from 0 to 20 (inclusive).</p> $\text{time (s)} = 4096 * \frac{2^{(\text{soft_start_time}+1)}}{\text{MCLK (Hz)}}$ |



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Register 15: GPIO Input Selection & Volume Configuration

| Bits | [7:6] | [5:4] | [3] | [2] | [1] | [0] |
|----------|-----------|-----------|----------|-------------|---------|-----------|
| Mnemonic | gpio_sel2 | gpio_sel1 | reserved | stereo_mode | ch1_vol | latch_vol |
| Default | 2'b00 | 2'b00 | 1'b1 | 1'b0 | 1'b0 | 1'b1 |

| Bit | Mnemonic | Description |
|-------|-------------|--|
| [7:6] | gpio_sel2 | Selects which input type will be selected when GPIOX = 1'b1 <ul style="list-style-type: none"> 2'd0: serial data (I2S/LJ/RJ) (default) 2'd1: SPDIF data 2'd2: reserved 2'd3: DSD data |
| [5:4] | gpio_sel1 | Selects which input type will be selected when GPIOX = 1'b0 <ul style="list-style-type: none"> 2'd0: serial data (I2S/LJ/RJ) (default) 2'd1: SPDIF data 2'd2: reserved 2'd3: DSD data |
| [3] | reserved | |
| [2] | stereo_mode | Maps channel 1 and channel 2 data across all 8 channels of the DAC. <ul style="list-style-type: none"> 1'b0: normal 8 channel operation (default) 1'b1: stereo mode operation where channel 1 is mapped to DACs 1, 3, 5 & 7, and channel 2 is mapped to DACs 2, 4, 6 & 8 |
| [1] | ch1_vol | Force all eight channels to use the volume coefficients from channel 1. <ul style="list-style-type: none"> 1'b0: each channel has independent volume control (default) 1'b1: all eight DAC channels use the channel 1 volume coefficient |
| [0] | latch_vol | Latches the data stores in registers 16-23 for use in calculating a new volume coefficient. Setting this bit to 0 will allow a customer to program all 8 channels individually and then update them all at once by setting this bit back to 1. <ul style="list-style-type: none"> 1'b0: disables latching of the volume control registers 1'b1: enables the volume control registers (default) |

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Register 16-23: Volume Control

| Bits | [7:0] |
|-------------|---------|
| Register 16 | volume1 |
| Register 17 | volume2 |
| Register 18 | volume3 |
| Register 19 | volume4 |
| Register 20 | volume5 |
| Register 21 | volume6 |
| Register 22 | volume7 |
| Register 23 | volume8 |
| Default | 8'd0 |

| Bit | Mnemonic | Description |
|-------|----------|--|
| [7:0] | volume1 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume2 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume3 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume4 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume5 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume6 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume7 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |
| [7:0] | volume8 | Default of 8'd0 -0dB to -127.5dB with 0.5dB steps |

Register 24-27: Master Trim

| Bits | [31:0] |
|----------|-------------|
| Mnemonic | master_trim |
| Default | 32'h7ffffff |

| Bit | Mnemonic | Description |
|--------|-------------|---|
| [31:0] | master_trim | A 32-bit signed value that sets the 0dB level for all volume controls. Defaults to full-scale (32'h7FFFFFFF). |

**Register 28-29: THD Compensation C2**

| | |
|----------|-------------|
| Bits | [15:0] |
| Mnemonic | thd_comp_c2 |
| Default | 16'd0 |

| Bit | Mnemonic | Description |
|--------|-------------|---|
| [15:0] | thd_comp_c2 | A 16-bit signed coefficient for correcting for the second harmonic distortion. Defaults to 16'd0. |

Register 30-31: THD Compensation C3

| | |
|----------|-------------|
| Bits | [15:0] |
| Mnemonic | thd_comp_c3 |
| Default | 16'd0 |

| Bit | Mnemonic | Description |
|--------|-------------|--|
| [15:0] | thd_comp_c3 | A 16-bit signed coefficient for correcting for the third harmonic distortion. Defaults to 16'd0. |

Register 32: Programmable FIR RAM Address

| | |
|----------|-----------------|
| Bits | [7:0] |
| Mnemonic | prog_coeff_addr |
| Default | 8'd0 |

| Bit | Mnemonic | Description |
|-------|-------------|--|
| [7] | coeff_stage | Selects which stage of the filter to write. <ul style="list-style-type: none"> 1'b0: selects stage 1 of the oversampling filter (default) 1'b1: selects stage 2 of the oversampling filter |
| [6:0] | coeff_addr | Selects the coefficient address when writing custom coefficients for the oversampling filter. |

Register 33-36: Programmable FIR RAM Data

| | |
|----------|-----------------|
| Bits | [31:0] |
| Mnemonic | prog_coeff_data |
| Default | 32'd0 |

| Bit | Mnemonic | Description |
|--------|------------|--|
| [31:0] | coeff_data | A 32-bit signed filter coefficient that will be written to the address defined in <i>prog_coeff_addr</i> . |

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Register 37: Programmable FIR Configuration

| Bits | [7] | [6:5] | [4] | [3] | [2] | [1] | [0] |
|----------|------------|----------|---------------|----------|-------------|---------|---------|
| Mnemonic | bypass_osf | reserved | filter_length | prog_ext | stage2_even | prog_we | prog_en |
| Default | 1'b0 | 2'b00 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|---------------|---|
| [7] | bypass_osf | Allows the use of an external 8x upsampling filter, bypassing the internal interpolating FIR filter. <ul style="list-style-type: none"> 1'b0: uses the built-in oversampling filter (default) 1'b1: uses an external upsampling filter, which requires data oversampled by 8x externally |
| [6:5] | reserved | |
| [4] | filter_length | Selects the filter length to be used in the first stage oversampling step. <ul style="list-style-type: none"> 1'b0: uses the standard 128-tap first stage filter when in fast roll-off mode (default) 1'b1: uses an extended 256-tap first stage filter at the expense of disabling oversampling on channels 3-8. This mode should only be used when in stereo operation and with channel mapping set appropriately |
| [3] | prog_ext | Enables programming the extended 256-tap coefficients. <ul style="list-style-type: none"> 1'b0: <i>prog_coeff_addr</i> maps to coefficients 0-127 (default) 1'b1: <i>prog_coeff_addr</i> maps to coefficients 128-255 |
| [2] | stage2_eve | Selects the symmetry of the stage 2 oversampling filter. <ul style="list-style-type: none"> 1'b0: Uses a sine symmetric filter (27 coefficients) (default) 1'b1: Uses a cosine symmetric filter (28 coefficients) |
| [1] | prog_we | Enables writing to the programmable coefficient RAM. <ul style="list-style-type: none"> 1'b0: Disables write signal to the coefficient RAM (default) 1'b1: Enables write signal to the coefficient RAM |
| [0] | prog_en | Enables the custom oversampling filter coefficients. <ul style="list-style-type: none"> 1'b0: Uses a built-in filter selected by <i>filter_shape</i> (default) 1'b1: Uses the coefficients programmed via <i>prog_coeff_data</i> |



Registers 38-41: DAC Channel Mapping

The DAC channel mapping registers are used to map the internal data path to the analog section. Any one of the 8 decoded input channels can be mapped to any of the 8 output DAC channels. By default, in1 will map to DAC1, etc. Each DAC has a 4-bit register that assigns the input channel.

- 4'd0: input 1 is used
- 4'd1: input 2 is used
- 4'd2: input 3 is used
- 4'd3: input 4 is used
- 4'd4: input 5 is used
- 4'd5: input 6 is used
- 4'd6: input 7 is used
- 4'd7: input 8 is used

Register 38: DAC 1-2 Mapping

| | | |
|----------|---------|---------|
| Bits | [7:4] | [3:0] |
| Mnemonic | ch2_map | ch1_map |
| Default | 4'd1 | 4'd0 |

Register 39: DAC 3-4 Mapping

| | | |
|----------|---------|---------|
| Bits | [7:4] | [3:0] |
| Mnemonic | ch4_map | ch3_map |
| Default | 4'd3 | 4'd2 |

Register 40: DAC 5-6 Mapping

| | | |
|----------|---------|---------|
| Bits | [7:4] | [3:0] |
| Mnemonic | ch6_map | ch5_map |
| Default | 4'd5 | 4'd4 |

Register 41: DAC 7-8 Mapping

| | | |
|----------|---------|---------|
| Bits | [7:4] | [3:0] |
| Mnemonic | ch8_map | ch7_map |
| Default | 4'd7 | 4'd6 |

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Register 42-45: Programmable NCO

| | |
|----------|---------|
| Bits | [31:0] |
| Mnemonic | nco_num |
| Default | 32'd0 |

| Bit | Mnemonic | Description |
|--------|----------|---|
| [31:0] | nco_num | <p>An unsigned 32-bit quantity that provides the ratio between MCLK and DATA_CLK. This value can be used to generate arbitrary DATA_CLK frequencies in master mode. A value of 0 disables this operating mode.</p> <p>Note: Master mode must still be enabled for the Sabre to drive the DATA_CLK and DATA1 pins. You must also select either serial mode or DSD mode in the <i>input_select</i> register to determine whether DATA_CLK should be driven alone (DSD mode) or both DATA_CLK and DATA1 should be driven (serial mode).</p> <ul style="list-style-type: none"> • 32'd0: disables NCO mode (default) • 32'dX: enables NCO mode <p>Note: NCO is determined by the following equation</p> $FSR = \frac{(nco_num * MCLK)}{2^{32}}$ |



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Register 46: ADC Configuration

| Bits | [7:6] | [5:4] | [3:2] | [1:0] |
|----------|------------------|-------------|----------------|---------|
| Mnemonic | adc_first_orderb | adc_clk_sel | adc_dither_enb | adc_pdb |
| Default | 2'b00 | 2'b00 | 2'b00 | 2'b00 |

| Bit | Mnemonic | Description |
|-------|------------------|--|
| [7:6] | adc_first_orderb | <p>Selects whether the ADC uses a first-order modulator or a second-order modulator in the analog section. [7] affects ADC2 while [6] affects ADC1.</p> <ul style="list-style-type: none"> 1'b0: uses a first order modulator providing the best performance (default) 1'b1: uses a second order modulator |
| [5:4] | adc_clk_sel | <p>Sets the clock dividing ratio for the ADC analog section. This setting also affects the decimation filter stages.</p> <ul style="list-style-type: none"> 2'd0: ADC_CLK = MCLK 2'd1: ADC_CLK = MCLK/2 2'd2: ADC_CLK = MCLK/4 2'd3: ADC_CLK = MCLK/8 |
| [3:2] | adc_dither_enb | <p>Allows the ADC dither to be disabled on a per ADC basis. [3] affects ADC2 while [2] affects ADC1.</p> <ul style="list-style-type: none"> 1'b0: uses TPDF shaped dither providing the best performance (default) 1'b1: disabled dither |
| [1:0] | adc_pdb | <p>Shuts down each ADC independently. [1] affects ADC2 while [0] affects ADC1. Note: GPIO must be configured as ADC mode for the ADC to function correctly.</p> <ul style="list-style-type: none"> 1'b0: shuts down the ADC (default) 1'b1: enables the ADC analog stage |

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Registers 47-52: ADC Filter Configuration

The SABRE DAC contains two decimation filters for filtering the ADC data. The filters are configurable via the ADC filter configuration registers. They are set as a low-pass filter by default. The low-pass filter is derived from commercial software.

Register 47-48: ADC Filter Configuration (ftr_scale)

| | |
|----------|----------------------|
| Bits | [15:0] |
| Mnemonic | <i>adc_ftr_scale</i> |
| Default | 16'd992 |

Register 49-50: ADC Filter Configuration (fbq_scale)

| | |
|----------|-----------------------|
| Bits | [15:0] |
| Mnemonic | <i>adc_fbq_scale1</i> |
| Default | 16'd1024 |

Register 51-52: ADC Filter Configuration (fbq_scale)

| | |
|----------|-----------------------|
| Bits | [15:0] |
| Mnemonic | <i>adc_fbq_scale2</i> |
| Default | 16'd1024 |

Register 53: Reserved

| | |
|----------|-----------------|
| Bits | [7:0] |
| Mnemonic | <i>reserved</i> |
| Default | 8'b00000000 |

Register 54: Reserved

| | | |
|----------|------------|-----------------|
| Bits | [7] | [6:0] |
| Mnemonic | DoP Bypass | <i>reserved</i> |
| Default | 1'b1 | 7'b1110000 |

| Bit | Mnemonic | Description |
|-------|-----------------|---|
| [7] | DoP Bypass | Selects whether the DAC will be able decode DoP audio data. <ul style="list-style-type: none"> 1'b0: enables the DoP transcoder 1'b1: disables the DoP transcoder (default) |
| [6:0] | <i>Reserved</i> | |

Register 55-56: Reserved

| | |
|----------|-----------------|
| Bits | [15:0] |
| Mnemonic | <i>reserved</i> |
| Default | 16'd0 |



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Register 57-61: Reserved

| | | |
|----------|----------|----------|
| Bits | [39:36] | [35:0] |
| Mnemonic | reserved | reserved |
| Default | 4'd4 | 36'd0 |

Register 62: +18dB Channel Gain

| | |
|----------|-------------------|
| Bits | [7:0] |
| Mnemonic | 18db_channel_gain |
| Default | 8'b00000000 |

| Bit | Mnemonic | Description |
|-----|------------|--|
| [7] | data8_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 8 1'b1: +18dB gain applied after volume control |
| [6] | data7_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 7 1'b1: +18dB gain applied after volume control |
| [5] | data6_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 6 1'b1: +18dB gain applied after volume control |
| [4] | data5_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 5 1'b1: +18dB gain applied after volume control |
| [3] | data4_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 4 1'b1: +18dB gain applied after volume control |
| [2] | data3_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 3 1'b1: +18dB gain applied after volume control |
| [1] | data2_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 2 1'b1: +18dB gain applied after volume control |
| [0] | data1_gain | <ul style="list-style-type: none"> 1'b0: No gain applied (default) to data channel 1 1'b1: +18dB gain applied after volume control |

Note: The +18dB gain only works in PCM mode and is applied prior to the channel mapping.

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Register 63: Auto Calibration and Modulator Configuration

| Bits | [7] | [6] | [5] | [4] | [3] | [2] | [1:0] |
|----------|----------|-----------|-------------|----------|----------|----------|----------|
| Mnemonic | calib_en | calib_sel | calib_latch | reserved | reserved | reserved | reserved |
| Default | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b1 | 2'b10 |

| Bit | Mnemonic | Description |
|-------|-------------|--|
| [7] | calib_en | Enables master trim calibration via the ADC input. <ul style="list-style-type: none"> 1'b0: Disables master trim auto calibration (default) 1'b1: Enables master trim auto calibration |
| [6] | calib_sel | Selects which ADC input is used for the master trim calibration. <ul style="list-style-type: none"> 1'b0: reserved 1'b1: Uses ADC2 (GPIO1) |
| [5] | calib_latch | Continues updating the calibration routine while set to 1'b1. |
| [4] | reserved | |
| [3] | reserved | |
| [2] | reserved | |
| [1:0] | reserved | |

Bits 3:2 of this register need to be written as 2'b10 to ensure the noise shaped modulator is stable under all conditions. If these bits are not set the noise shaped modulator can be unstable. Although the ES9028PRO will continue to function normally the noise floor will be degraded.



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Register 64 (Read-Only): Chip ID and Status

| Bits | [7:2] | [1] | [0] |
|----------|-----------|-----------------|-------------|
| Mnemonic | chip_id | automute_status | lock_status |
| Default | 6'b101000 | 1'b0 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|-----------------|--|
| [7:2] | chip_id | Determines the chip identification <ul style="list-style-type: none"> 6'b101000: ES9028PRO |
| [1] | automute_status | Indicator for when automute has become active. <ul style="list-style-type: none"> 1'b0: Automute condition is inactive 1'b1: Automute condition has been flagged and is active |
| [0] | lock_status | Indicator for when the DPLL is locked (when in slave mode) or 1'b1 when the Sabre is the master <ul style="list-style-type: none"> 1'b0: DPLL is not locked to the incoming audio sample rate (which could mean that no audio input is present, the lock has not completed, or the Sabre is unable to lock due to clock jitter or drift) 1'b1: DPLL is locked to the incoming audio sample rate, or the Sabre is in master mode, 128fs_mode or NCO mode mode |

Register 65 (Read-Only): GPIO Readback

| Bits | [7:4] | [3] | [2] | [1] | [0] |
|----------|----------|-------|-------|-------|-------|
| Mnemonic | reserved | gpio4 | gpio3 | gpio2 | gpio1 |
| Default | 4'b0000 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|----------|--------------------------------------|
| [7:4] | reserved | |
| [3] | gpio4 | Contains the state of the GPIO4 pin. |
| [2] | gpio3 | Contains the state of the GPIO3 pin. |
| [1] | gpio2 | Contains the state of the GPIO2 pin. |
| [0] | gpio1 | Contains the state of the GPIO1 pin. |

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Register 66-69 (Read-Only): DPLL Number

| | |
|----------|----------|
| Bits | [31:0] |
| Mnemonic | dp11_num |
| Default | 32'd0 |

| Bit | Mnemonic | Description |
|--------|----------|---|
| [31:0] | dp11_num | <p>Contains the ratio between the MCLK and the audio clock rate once the DPLL has acquired lock. This value is latched on reading the LSB, so register 66 must be read first to acquire the latest DPLL value. The value is latched on LSB because the DPLL number can be changing as the I2C transactions are performed.</p> $FSR = \frac{(dp11_num * MCLK)}{2^{32}}$ |

Register 70-93: (Read-Only): SPDIF Channel Status/User Status

| | |
|----------|--------------|
| Bits | [191:0] |
| Mnemonic | spdif_status |
| Default | 192'd0 |

| Bit | Mnemonic | Description |
|---------|--------------|---|
| [191:0] | spdif_status | Contains either the SPDIF channel status (table shown below) or the SPDIF user bits. This selection can be made via register 1 (user_bits). |



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| SPDIF CHANNEL STATUS – Consumer configuration | | | | | | | | |
|---|---|----------|--|----------|--|--------------------------------|-------------------|---|
| Address Offset | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] |
| 0 | Reserved | Reserved | 0:2Channel 1:4Channel | Reserved | 0:No-Preemph 1:Preemph | 0:CopyRight 1:Non-CopyRight | 0:Audio 1:Data | 0:Consumer 1:Professional |
| 1 | Category Code 0x00: General 0x01:Laser-Optical 0x02:D/D Converter 0x03:Magnetic 0x04:Digital Broadcast 0x05:Musical Instrument 0x06:Present A/D Converter 0x08:Solid State Memory 0x16:Future A/D Converter 0x19:DVD 0x40:Experimental | | | | | | | |
| 2 | Channel Number 0x0: Don't Care 0x1: A (Left) 0x2: B (Right) 0x3: C 0x4: D 0x5: E 0x6: F 0x7: G 0x8: H 0x9: I 0xA: J 0xB: K 0xC: L 0xD: M 0xE: N 0xF: O | | | | Source Number 0x0:Don't Care 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: G 0x8: 8 0x9: 9 0xA: 10 0xB: 11 0xC: 12 0xD: 13 0xE: 14 0xF: 15 | | | |
| 3 | Reserved | Reserved | Clock Accuracy 0x0:Level 2 ±1000ppm 0x1:Level 1 ±50ppm 0x2:Level 3 variable pitch shifted | | Sample Frequency 0x0: 44.1k 0x2: 48k 0x3: 32k 0x4: 22.05k 0x6: 24k 0x8: 88.2k 0xA: 96k 0xC: 176.4k 0xE: 192k | | | |
| 4 | Reserved | Reserved | Reserved | Reserved | Word Length: If Word Field Size=0 If Word Field Size = 1 000=Not indicated 000=Not indicated 100 = 23bits 100 = 19bits 010 = 22bits 010 = 18bits 110 = 21bits 110 = 17bits 001 = 20bits 001 = 16bits 101 = 24bits 101 = 20bits | | | Word Field Size 0:Max 20bits 1:Max 24bits |
| 5-23 | Reserved | | | | | | | |

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| SPDIF CHANNEL STATUS – Professional configuration | | | | | | | | |
|---|--|--|--|---|--|------------------------|---|--------------------------------------|
| Address Offset | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] |
| 0 | sampling frequency: 00: not indicated (or see byte 4) 10: 48 kHz 01: 44.1 kHz 11: 32 kHz | | lock: 0: locked 1: unlocked | emphasis: 000: Emphasis not indicated 001: No emphasis 011: CD-type emphasis 111: J-17 emphasis | | 0:Audio 1:Non-audio | | 0:Consumer 1: Professional |
| 1 | User bit management: 0000: no indication 1000: 192-bit block as channel status 0100: As defined in AES18 1100: user-defined 0010: As in IEC60958-3 (consumer) | | | | Channel mode: 0000: not indicated (default to 2 ch) 1000: 2 channel 0100: 1 channel (monophonic) 1100: primary / secondary 0010: stereo 1010: reserved for user applications 0110: reserved for user applications 1110: SCDSR (see byte 3 for ID) 0001: SCDSR (stereo left) 1001: SCDSR (stereo right) 1111: Multichannel (see byte 3 for ID) | | | |
| 2 | alignment level: 00: not indicated 10: –20dB FS 01: –18.06dB FS | | Source Word Length: If max = 20bits If max = 24bits 000=Not indicated 000=Not indicated 100 = 23bits 100 = 19bits 010 = 22bits 010 = 18bits 110 = 21bits 110 = 17bits 001 = 20bits 001 = 16bits 101 = 24bits 101 = 20bits | | Use of aux sample word: 000: not defined, audio max 20 bits 100: used for main audio, max 24 bits 010: used for coord, audio max 20 bits 110: reserved | | | |
| 3 | Channel identification: if bit 7 = 0 then channel number is 1 plus the numeric value of bits 0-6 (bit reversed). if bit 7 = 1 then bits 4–6 define a multichannel mode and bits 0–3 (bit reversed) give the channel number within that mode. | | | | | | | |
| 4 | fs scaling: 0: no scaling 1: apply factor of 1 / 1.001 to value | Sample frequency (fs): 0000: not indicated 0001: 24kHz 0010: 96kHz 1001: 22.05kHz 1010: 88.2kHz 1011: 176.4kHz 0011: 192kHz 1111: User defined | | | Reserved | | DARS (Digital audio reference signal): 00: not a DARS 01: DARS grade 2 (±10ppm) 10: DARS grade 1 (±1ppm) 11: Reserved | |
| 5 | Reserved | | | | | | | |
| 6-9 | alphanumerical channel origin: four-character label using 7-bit ASCII with no parity. Bits 55, 63, 71, 79 = 0. | | | | | | | |
| 10-13 | alphanumerical channel destination: four-character label using 7-bit ASCII with no parity. Bits 87, 95, 103, 111 = 0. | | | | | | | |
| 14-17 | local sample address code: 32-bit binary number representing the sample count of the first sample of the channel status block. | | | | | | | |
| 18-21 | time of day code: 32-bit binary number representing time of source encoding in samples since midnight | | | | | | | |
| 22 | reliability flags 0: data in byte range is reliable 1: data in byte range is unreliable | | | | | | | |
| 23 | CRCC 00000000: not implemented X: error check code for bits 0–183 | | | | | | | |



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Register 94-99 (Read-Only): Reserved

Register 100 (Read-Only): Input Selection

| Bits | [7:4] | [3] | [2] | [1] | [0] |
|----------|----------|-----------|--------------|------------|------------|
| Mnemonic | reserved | dop_valid | spdif_select | i2s_select | dsd_select |
| Default | 4'b0000 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

| Bit | Mnemonic | Description |
|-------|--------------|--|
| [7:4] | reserved | |
| [3] | dop_valid | Contains the status of the DoP decoder. <ul style="list-style-type: none"> 1'b0: The DoP decoder has not detected a valid DoP signal. 1'b1: The DoP decoder has detected a valid DoP signal on the I2S or SPDIF inputs. |
| [2] | spdif_select | Contains the status of the SPDIF decoder. <ul style="list-style-type: none"> 1'b0: The SPDIF decoder has been unable to decode a valid SPDIF frame. 1'b1: The SPDIF decoder has decoded a sequence of valid SPDIF frames. |
| [1] | i2s_select | Contains the status of the I2S decoder. <ul style="list-style-type: none"> 1'b0: The I2S decoder has not found a valid frame clock or bit clock. 1'b1: The I2S decoder has detected a valid frame clock and bit clock arrangement. |
| [0] | dsd_select | Contains the status of the DSD decoder. <ul style="list-style-type: none"> 1'b0: The DSD decoder is not being used. 1'b1: The DSD decoder is being used as a fallback option if I2S and SPDIF have both failed to decode their respective input signals. |

Register 101-109: Reserved

Register 110-112: ADC1 GPIO2 (READ ONLY)

| | |
|----------|----------------|
| Bits | [23:0] |
| Mnemonic | adc_fbq_scale2 |
| Default | 24'd0 |

Register 113-115: ADC2 GPIO1 (READ ONLY)

| | |
|----------|----------------|
| Bits | [23:0] |
| Mnemonic | adc_fbq_scale2 |
| Default | 24'd0 |

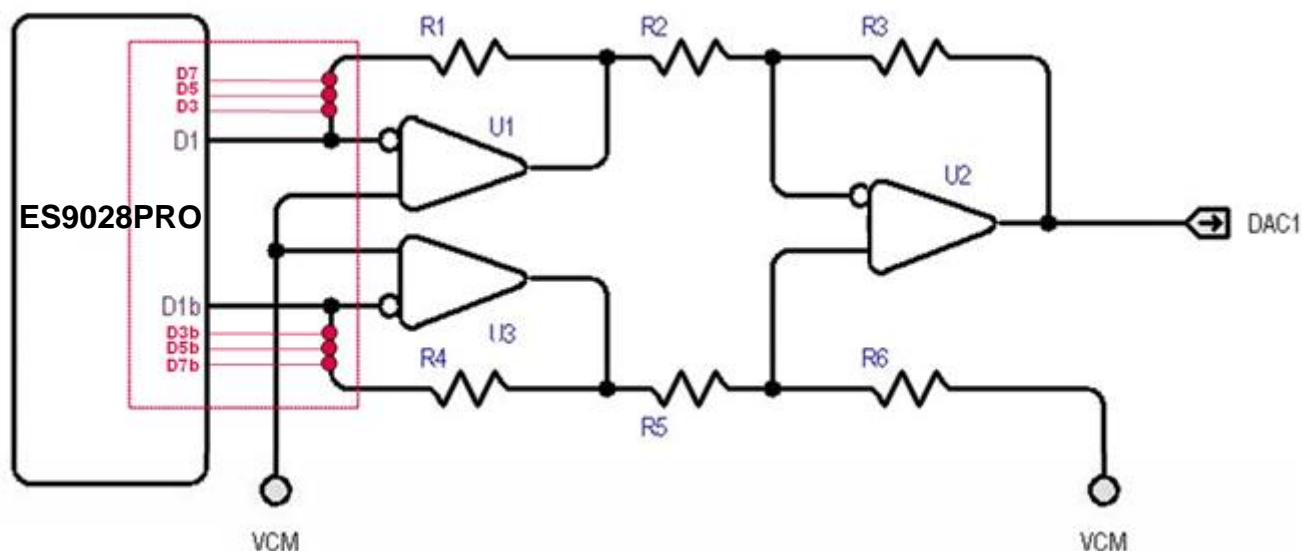
ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



APPLICATION DIAGRAMS

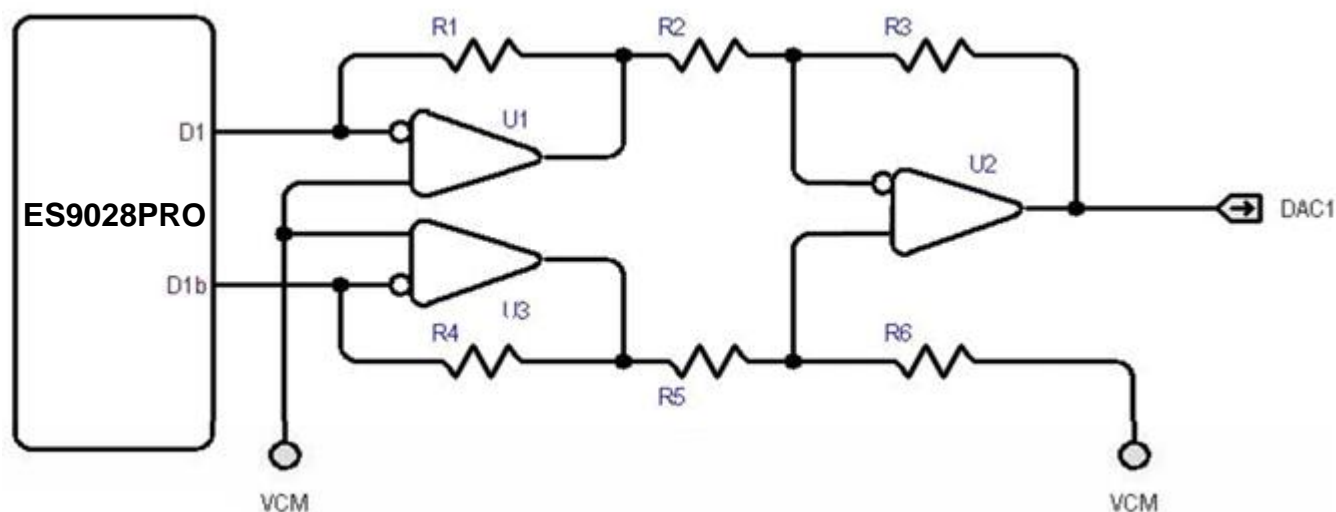
ES9028PRO Stereo Quad-Differential Output, Current Mode Operation

SABRE DAC in stereo “quad-differential” current mode
(DNR: 133dB, THD: -120dB)



ES9028PRO 8-Channel Output, Current-Mode Operation

SABRE DAC in 8-Channel differential in current-mode
(DNR: 129dB, THD: -120dB)





ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING |
|--|---------------------------|
| Positive Supply Voltage (VCCA, AVDD, AVCC) | +4.7V with respect to GND |
| Positive Supply Voltage (DVDD, VDD_L, VDD_R) | +1.8V with respect to GND |
| DAC Output Voltage Range | GND < Vout < AVCC |
| Voltage Range for 5V Tolerant pins (AVDD=3.3V) | −0.5V to +5.5V |
| Voltage Range for Digital Input pins | −0.5V to (AVDD + 0.5V) |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature | +125°C |
| ESD Protection | |
| Human Body Model (HBM) | 2000V |
| Machine Model (MM) | 200V |
| Charged Device Model (CDM) | 500V |

WARNING: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS |
|----------------------------------|----------------|---|
| Operating Temperature | T _A | 0°C to +70°C |
| Analog Power Supply Voltage | VDD_L, VDD_R | +1.2V ± 5%, 82mA nominal (Note 1) |
| Digital Core Supply Voltage | DVDD | |
| Analog Reference Supply Voltage | AVCC_L, AVCC_R | +3.3V ± 5%, 47mA nominal (Note 1) |
| Oscillator Power Supply Voltage | VCCA | +3.3V ± 5%, 3mA nominal (Note 1) |
| Digital I/O Power Supply Voltage | AVDD | +3.3V ± 5%, <1mA nominal (Note 1) +1.8V ± 5% |

Note 1: f_s = 48kHz, MCLK = 40MHz, I²S input, all GPIOs set to input and pulled low

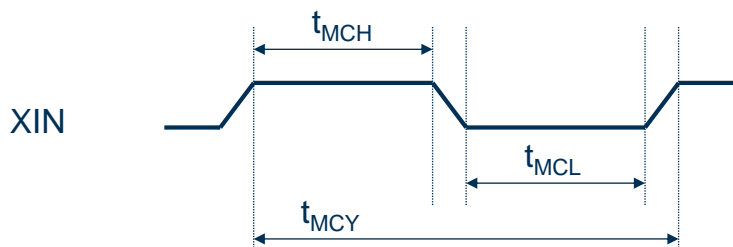
DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Minimum | Maximum | Unit | Comments |
|-----------------|---------------------------|----------------|---------|------|-------------------------|
| V _{IH} | High-level input voltage | AVDD / 2 + 0.4 | | V | |
| V _{IL} | Low-level input voltage | | 0.4 | V | |
| V _{OH} | High-level output voltage | AVDD - 0.2 | | V | I _{OH} = 100μA |
| V _{OL} | Low-level output voltage | | 0.2 | V | I _{OL} = 100μA |

ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

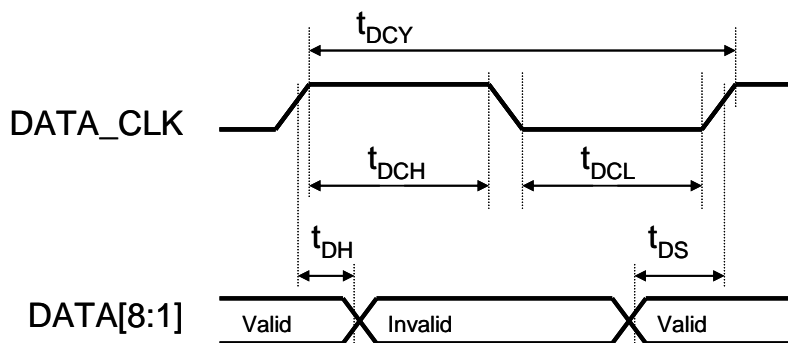


XIN Timing



| Parameter | Symbol | Min | Max | Unit |
|----------------------|-----------|-------|-------|------|
| XIN pulse width high | T_{MCH} | 4.5 | | ns |
| XIN pulse width low | T_{MCL} | 4.5 | | ns |
| XIN cycle time | T_{MCY} | 10 | | ns |
| XIN duty cycle | | 45:55 | 55:45 | |

Audio Interface Timing

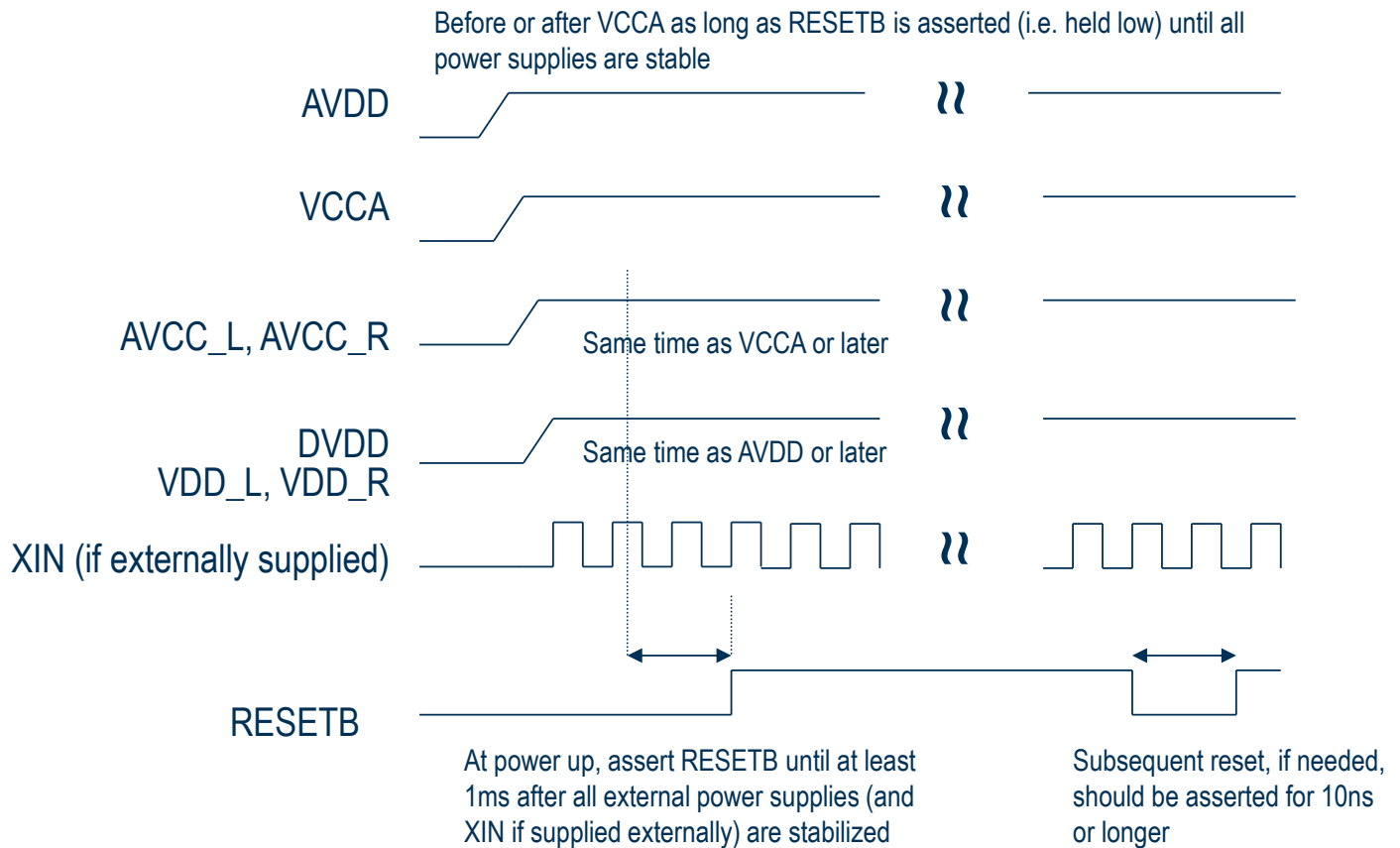


| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-------|-------|------|
| DATA_CLK pulse width high | t_{DCH} | 4.5 | | ns |
| DATA_CLK pulse width low | t_{DCL} | 4.5 | | ns |
| DATA_CLK cycle time | t_{DCY} | 10 | | ns |
| DATA_CLK duty cycle | | 45:55 | 55:45 | |
| DATA set-up time to DATA_CLK rising edge | t_{DS} | 2 | | ns |
| DATA hold time to DATA_CLK rising edge | t_{DH} | 2 | | ns |



ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

Recommended Power-Up Sequence



The ES9028PRO must be reset after power-up to ensure correct operation. Reset can be performed using a reset controller in some configurations or via a system software reset. The active-LOW reset pin provides a high input-impedance with no internal pull-up or pull-down. To reset the ES9028PRO, the reset input should be pulled low for a minimum of 1ms after all external power supplies (and XIN if supplied externally) are stabilized. Following the reset signal, the input can be held high indefinitely.

ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

1. $T_A = 25^\circ\text{C}$, $AVCC = +3.3\text{V}$, $VDD = +1.2\text{V}$, $f_s = 44.1\text{kHz}$, $MCLK = 27\text{MHz}$ and 32-bit data
2. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
3. THD+N: un-weighted over 20Hz-20kHz bandwidth

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-------------------|--|-----------------------------|----------|
| Resolution | | | 32 | | Bits |
| XIN frequency | | | | 100 | MHz |
| MCLK (PCM normal mode) | Asynchronous mode Synchronous mode | >128FSR 128FSR | | $\frac{XIN}{2^{clk_gear}}$ | Hz |
| MCLK (PCM OSF bypass mode) | Asynchronous mode Synchronous mode | 24FSR 16FSR | | | |
| MCLK (DSD mode) | Asynchronous mode Synchronous mode | 3FSR 2FSR | | | |
| MCLK (SPDIF mode) | | 386FSR | | | |
| FSR (PCM normal mode) | Asynchronous mode Synchronous mode | | | 384 768 | kHz |
| FSR (PCM OSF bypass mode) | | | | 1.536 | MHz |
| FSR (DSD mode) | Asynchronous mode Synchronous mode | | | 11.3 22.6 | MHz |
| FSR (SPDIF mode) | | | | 192 | kHz |
| DYNAMIC PERFORMANCE | | | | | |
| DNR (mono differential current mode) | | -60dBFS | | 135 | dB-A |
| DNR (stereo differential current mode) | | -60dBFS | | 133 | dB-A |
| DNR (8-Ch differential current mode) | | -60dBFS | | 129 | dB-A |
| THD+N (differential current mode) | | 0dBFS | | -120 | dB |
| ANALOG OUTPUT (per + or - pin of each differential DAC output pair) | | | | | |
| Output impedance (R_{DAC}) | | | $806 \pm 14\%$ | | Ω |
| Voltage mode output range (V_{OPP}) | Full-scale out | | $0.924 \times AVCC$ | | Vp-p |
| Voltage mode output offset (V_{OCM}) | Bipolar zero out | | $AVCC / 2$ | | V |
| Current mode output range | Full-scale out | | $1000 \times V_{OPP} / R_{DAC}$ | | mAp-p |
| Current mode output offset | Bipolar zero out to virtual ground held at V_G (V) | | $1000 \times (V_{OPP} - V_G) / R_{DAC}$ | | mA |
| Digital Filter Performance | | | | | |
| De-emphasis error | | | | ± 0.2 | dB |
| Mute Attenuation | | | 127 | | dB |
| IIR Filter Characteristics | | | | | |
| Pass band (-3dB) | iir_bw=0 iir_bw=1 iir_bw=2 iir_bw=3 | | 47 x $f_s/44100$ 50 x $f_s/44100$ 60 x $f_s/44100$ 70 x $f_s/44100$ | | kHz |
| Stop band attenuation | | | 18 | | dB/oct |



ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

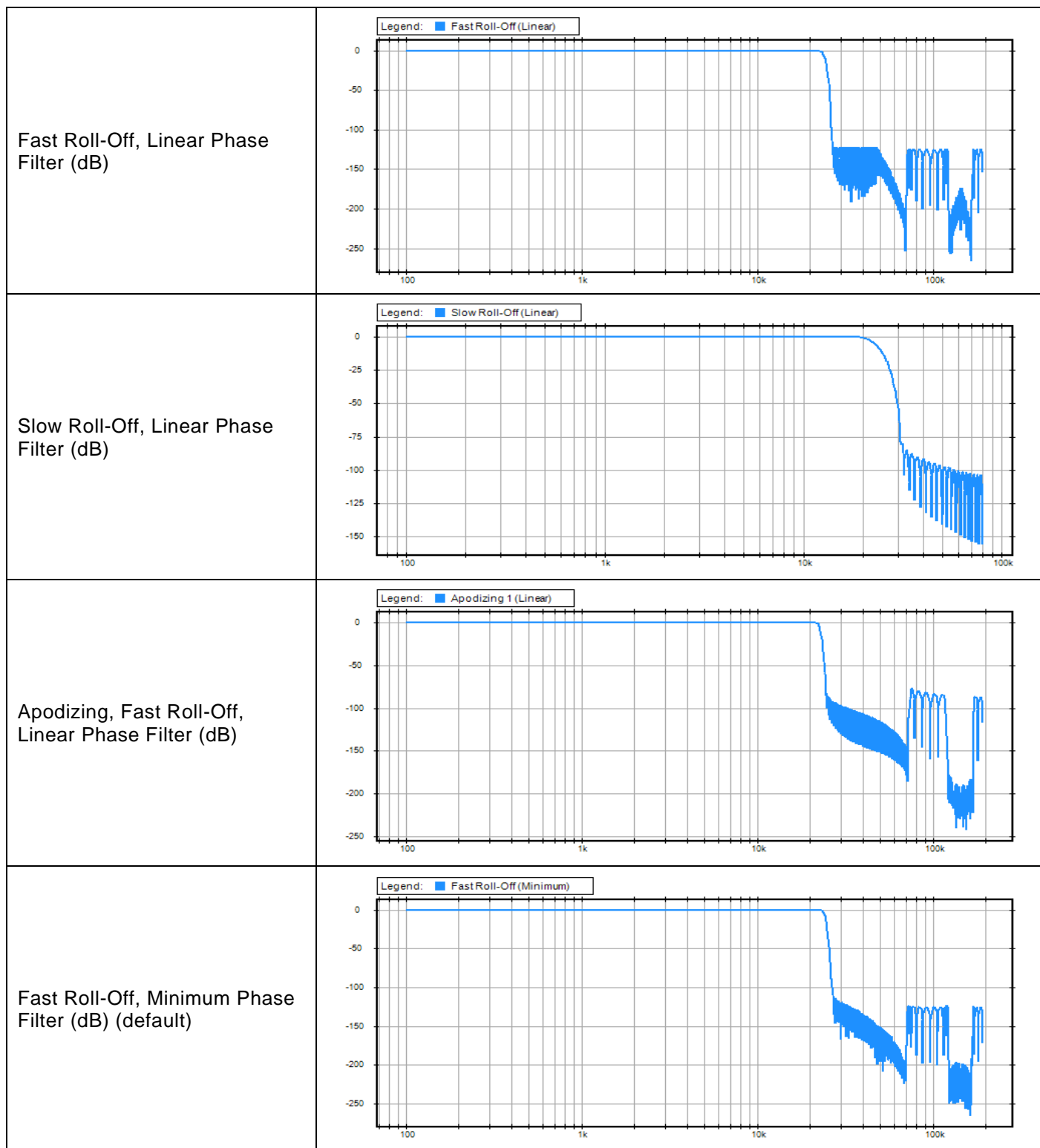
ANALOG PERFORMANCE (Cont'd)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|----------------------|--------------------|--------------|--------------------|------|
| PCM Filter Characteristics (Fast Roll Off, Linear Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.002\text{dB}$ | | | $0.453 \times f_s$ | Hz |
| | | -3dB | | | $0.484 \times f_s$ | Hz |
| Stop band | | $< -120\text{dB}$ | $0.55 \times f_s$ | | | Hz |
| Group Delay | | | | $35 / f_s$ | | s |
| PCM Filter Characteristics (Slow Roll Off, Linear Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.01\text{dB}$ | | | $0.357 \times f_s$ | Hz |
| | | -3dB | | | $0.450 \times f_s$ | Hz |
| Stop band | | $< -82\text{dB}$ | $0.639 \times f_s$ | | | Hz |
| Group Delay | | | | $8.75 / f_s$ | | s |
| PCM Filter Characteristics (Apodizing, Fast Roll Off, Linear Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.075\text{dB}$ | | | $0.409 \times f_s$ | Hz |
| | | -3dB | | | $0.461 \times f_s$ | Hz |
| Stop band | | $< -80\text{dB}$ | $0.50 \times f_s$ | | | Hz |
| | | $< -100\text{dB}$ | $0.66 \times f_s$ | | | Hz |
| Group Delay | | | | $35 / f_s$ | | s |
| PCM Filter Characteristics (Fast Roll Off, Minimum Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.005\text{dB}$ | | | $0.453 \times f_s$ | Hz |
| | | -3dB | | | $0.491 \times f_s$ | Hz |
| Stop band | | $< -67.5\text{dB}$ | $0.531 \times f_s$ | | | Hz |
| | | $< -100\text{dB}$ | $0.547 \times f_s$ | | | Hz |
| Group Delay | | | | $5.4 / f_s$ | | s |
| PCM Filter Characteristics (Slow Roll Off, Minimum Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.015\text{dB}$ | | | $0.363 \times f_s$ | Hz |
| | | -3dB | | | $0.435 \times f_s$ | Hz |
| Stop band | | $< -97\text{dB}$ | $0.634 \times f_s$ | | | Hz |
| Group Delay | | | | $3.5 / f_s$ | | s |
| PCM Filter Characteristics (Hybrid, Fast Roll Off, Minimum Phase) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.01\text{dB}$ | | | $0.404 \times f_s$ | Hz |
| | | -3dB | | | $0.430 \times f_s$ | Hz |
| Stop band | | $< -94.5\text{dB}$ | $0.504 \times f_s$ | | | Hz |
| | | $< -106\text{dB}$ | $0.513 \times f_s$ | | | Hz |
| Group Delay | | | | $18.5 / f_s$ | | s |
| PCM Filter Characteristics (Brickwall) | | | | | | |
| Pass band Ripple and Bandwidth | | $\pm 0.015\text{dB}$ | | | $0.435 \times f_s$ | Hz |
| | | -3dB | | | $0.451 \times f_s$ | Hz |
| Stop band | | $< -100\text{dB}$ | $0.50 \times f_s$ | | | Hz |
| Group Delay | | | | $35 / f_s$ | | s |

ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

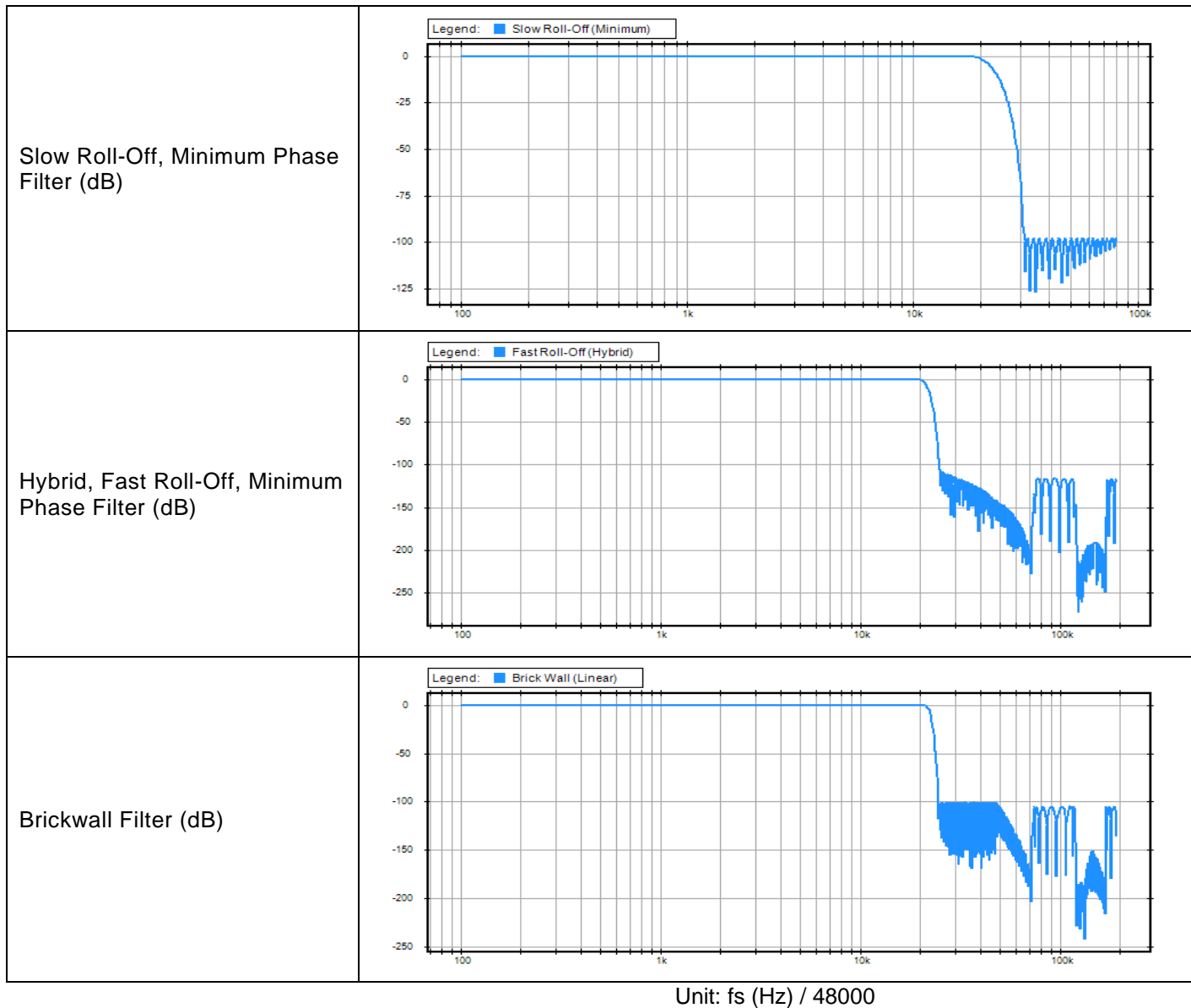


PCM FILTER FREQUENCY RESPONSE





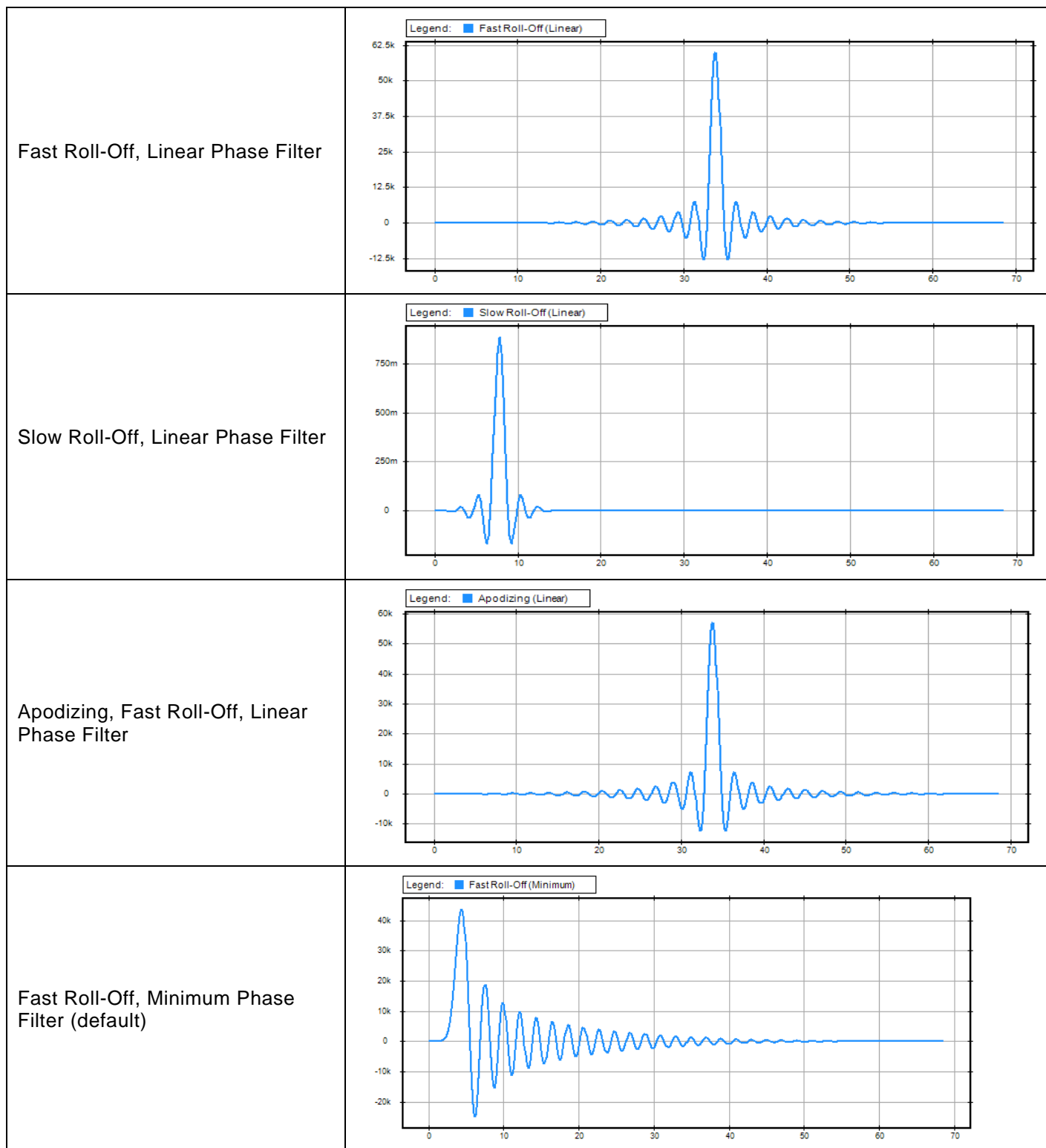
ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

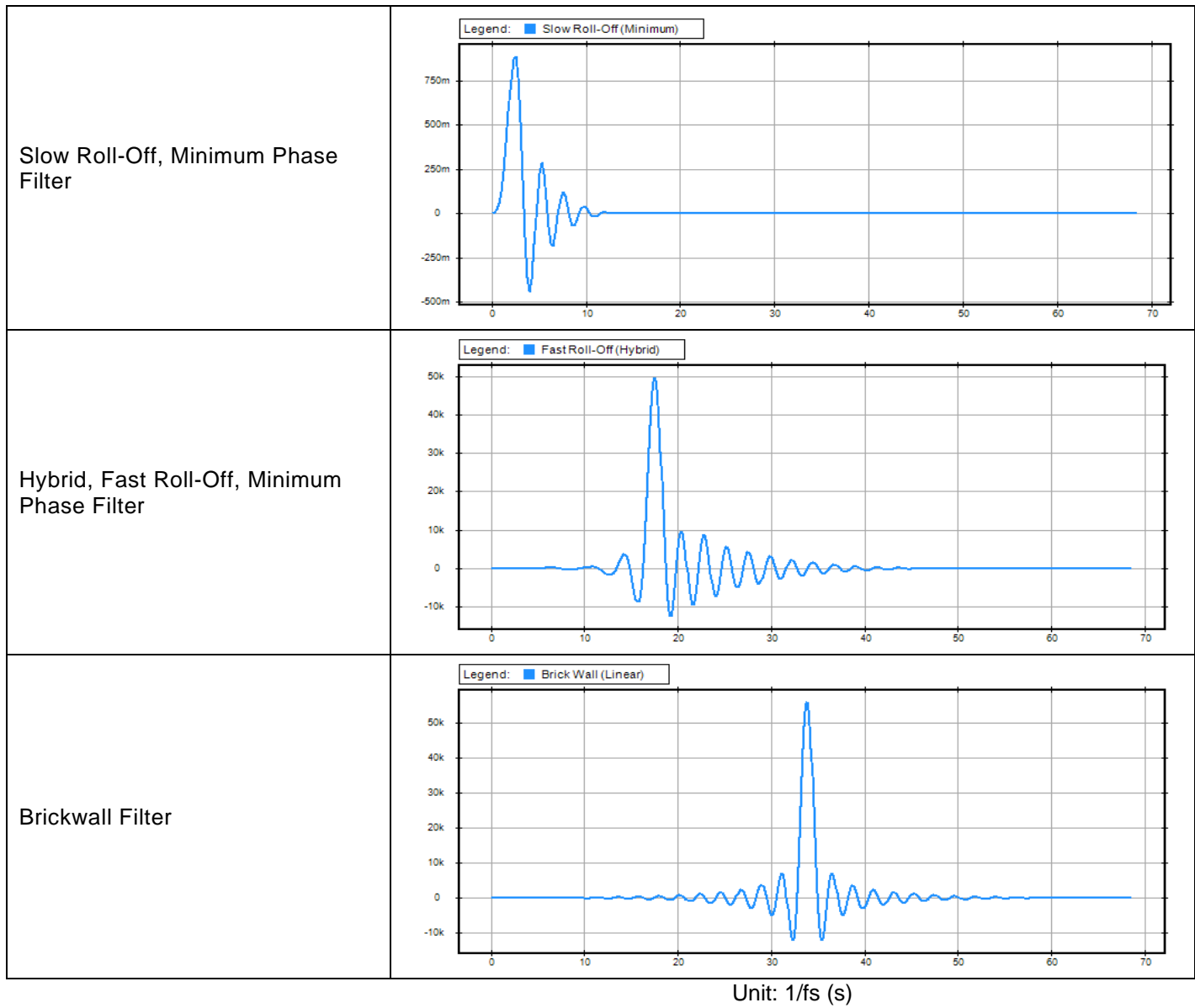


PCM FILTER IMPULSE RESPONSE





ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



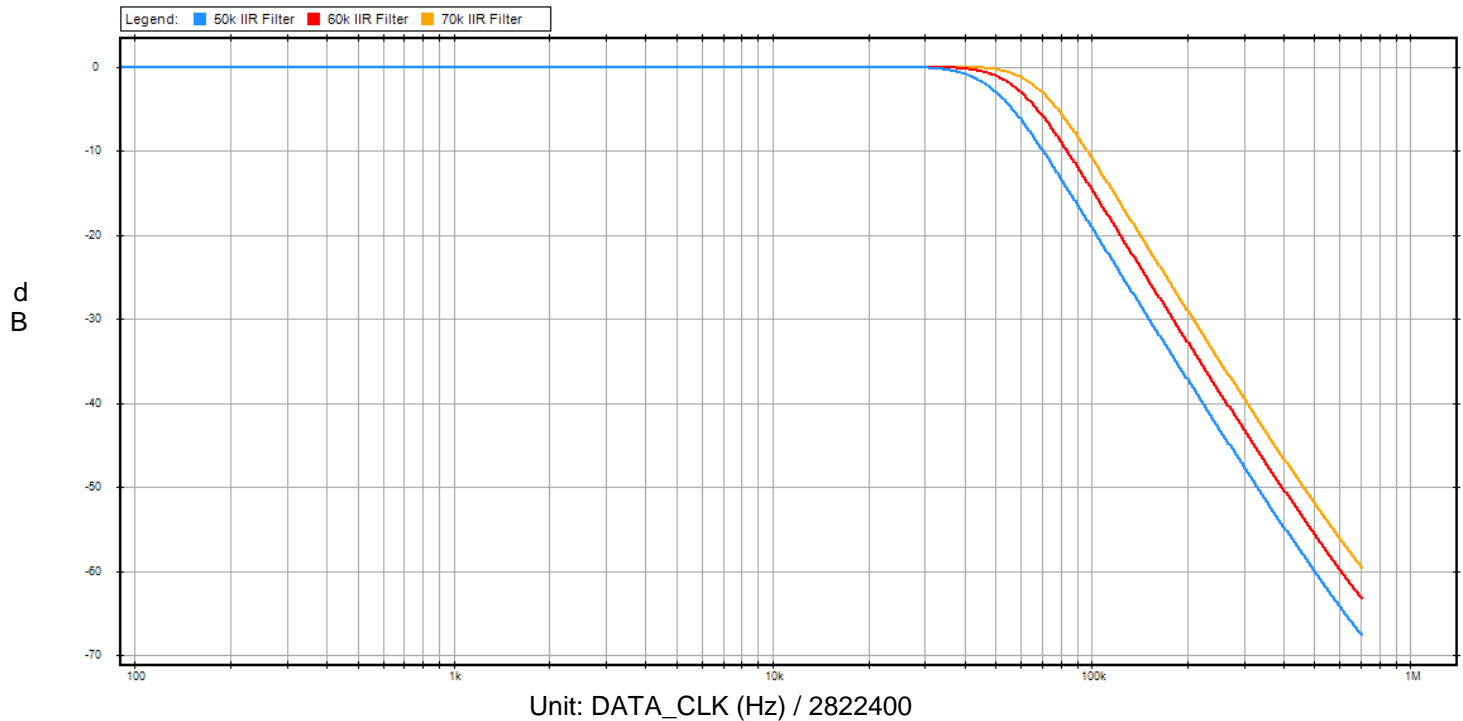
ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



IIR FILTER RESPONSE

The default IIR setting is intended for use in PCM mode only. It has been designed to work with the FIR filter. In DSD mode the FIR filter is bypassed, and the frequency response is defined entirely by the 8x IIR filter.

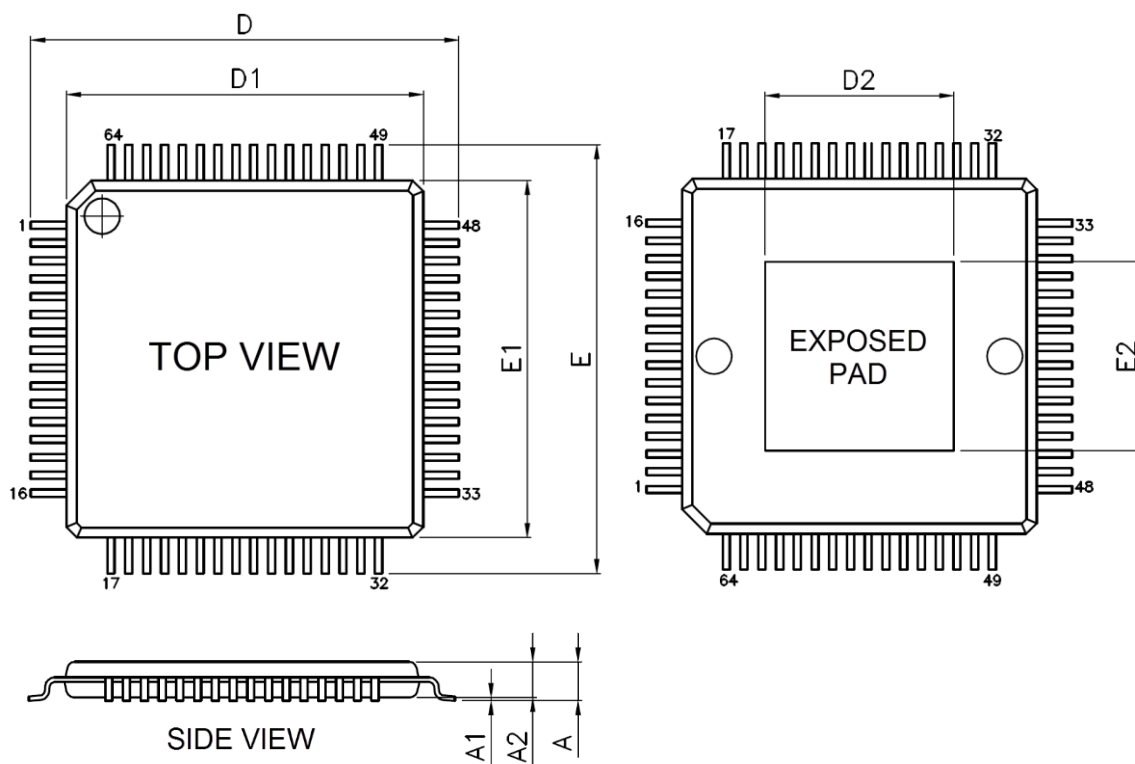
3 IIR filter profiles are included for use in DSD mode.





ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

64-Pin eTQFP Mechanical Dimensions



| Symbol | Description | Millimeters | | |
|--------|---------------------------|-------------|----------|-------|
| | | Min. | Nom. | Max. |
| D | Lead-to Lead, X-axis | 11.75 | 12.00 | 12.25 |
| D1 | Package's Outside, X-axis | 9.90 | 10.00 | 10.10 |
| E | Lead-to Lead, Y-axis | 11.75 | 12.00 | 12.25 |
| E1 | Package's Outside, Y-axis | 9.90 | 10.00 | 10.10 |
| A | Package Height | | | 1.20 |
| A1 | Board Standoff | 0.05 | 0.10 | 0.15 |
| A2 | Package Thickness | 0.95 | 1.00 | 1.05 |
| b | Lead Width | 0.17 | 0.22 | 0.27 |
| | Lead Pitch | | 0.50 BSC | |
| | No. of Leads in X-axis | | 16 | |
| | No. of Leads in Y-axis | | 16 | |
| | No. of Leads Total | | 64 | |
| | Package Type | | eTQFP | |

| PAD SIZE | D2 | | E2 | |
|----------|------|------|------|------|
| | Min. | Max. | Min. | Max. |
| | 5.13 | 5.48 | 5.13 | 5.48 |

ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.

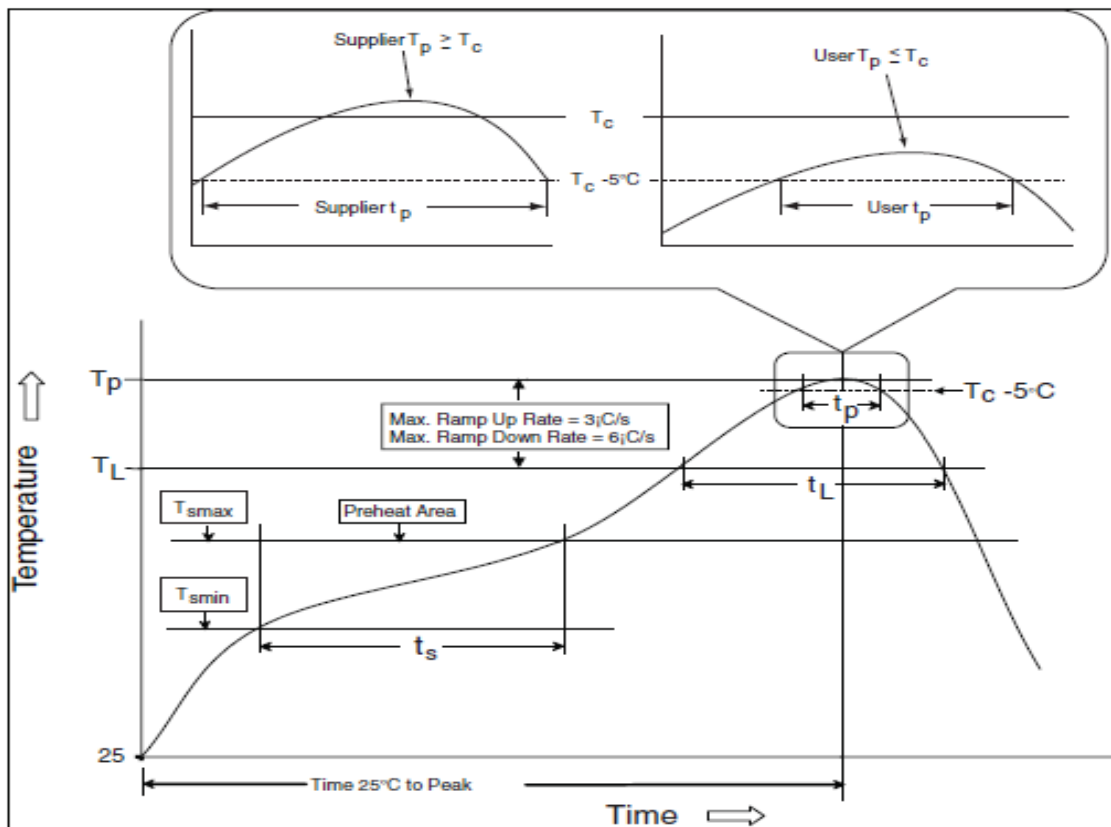
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (*Table RPC-2*). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (*Table RPC-2*).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:

Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.



ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC

Table RPC-1 Classification reflow profile

| Profile Feature | Pb-Free Assembly |
|--|---|
| Preheat/Soak | |
| Temperature Min (T _{min}) | 150°C |
| Temperature Max (T _{max}) | 200°C |
| Time (ts) from (T _{min} to T _{max}) | 60-120 seconds |
| Ramp-up rate (TL to Tp) | 3°C / second max. |
| Liquidous temperature (TL) | 217°C |
| Time (tL) maintained above TL | 60-150 seconds |
| Peak package body temperature (Tp) | For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2. |
| Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1 | 30* seconds |
| Ramp-down rate (Tp to TL) | 6°C / second max. |
| Time 25°C to peak temperature | 8 minutes max. |
| * Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. | |

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within $\pm 2^\circ\text{C}$ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process - Classification Temperatures (Tc)

| Package Thickness | Volume mm ³ , <350 | Volume mm ³ , 350 to 2000 | Volume mm ³ , >2000 |
|-------------------|-------------------------------|--------------------------------------|--------------------------------|
| <1.6 mm | 260°C | 260°C | 260°C |
| 1.6 mm - 2.5 mm | 260°C | 250°C | 245°C |
| >2.5 mm | 250°C | 245°C | 245°C |

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ES9028PRO 32-Bit HyperStream® II 8-Channel Audio DAC



ORDERING INFORMATION

| Part Number | Description | Package |
|-------------|--|----------|
| ES9028PRO | SABRE PRO 32-Bit Hyperstream® II 8-Channel Audio DAC | 64-eTQFP |

Revision History

| Rev. | Date | Notes |
|------|-------------------|---|
| 0.1 | December 22, 2015 | Initial release |
| 1.0 | April 21, 2016 | Revision 1.0 release |
| 1.1 | April 26, 2016 | Added description of DSD over PCM (DoP) support. |
| 2.0 | July 7, 2016 | Revision 2.0 release |
| 2.02 | July 18, 2016 | Update power consumption table |
| 2.1 | August 22, 2016 | Correct register #6[6] to deemph_bypass Add notes that multi-byte registers use little-endian ordering |
| 2.5 | October 13, 2016 | Updated Register #54[7] Updated Asynchronous Mode to 128Fs |
| 2.6 | November 22, 2016 | Updated Chip ID |
| 2.7 | March 8, 2017 | Updated Register #63 [3:2] |
| 2.8 | April 21, 2017 | Fixed typo for note under Register #63 |
| 2.9 | August 25, 2017 | Updated front page removed “mobile” in the Benefits |
| 3.0 | November 28, 2017 | Removed ESS logo from pin diagram |
| 3.1 | December 1, 2017 | Renumber SPDIF inputs in pin description to match table on page 6 |
| 3.2 | March 14, 2018 | Add note for VDD_L, VDD_R and DVDD internal connection |
| 3.3 | March 29, 2018 | Added notes for FIR and IIR filter usage to Register 7 description. Added additional description to IIR filter response section. |
| 3.4 | May 2, 2018 | Corrected example code used to load custom filter. |
| 3.5 | March 5, 2019 | Updated SABRE®, Hyperstream®II, SABRE SOUND®. Updated Register #63 [3:2] |
| 3.6 | July 6, 2020 | Corrected Xin pin layout |

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