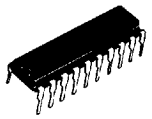
LC7881, 7881M



CMOS LSI

16-bit D/A Converter for Digital Audio

Overview

The LC7881 16-bit CMOS D/A converter (DAC) uses dynamic level shift, combining resistance strings and pulse-width modulation (PWM) with level shifts. Two D/A conversion channels are built in, and the output to the right and left channels is in-phase, making this device ideal for digital audio applications. Further, deglitching circuitry is not required.

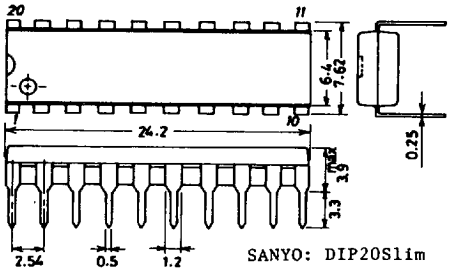
Features

- Compatible with 2's complement code
- 2 D/A converter channels built in
- In-phase output to the CH1 and CH2
- 176.4kHz (max.) conversion frequency (with 4 times oversampling capability)
- No diglitch circuit required
- Si-gate CMOS process for low-power operation
- Single 5V power supply

Maximum Ratings at Ta = 25°C, V_{SS} = 0V

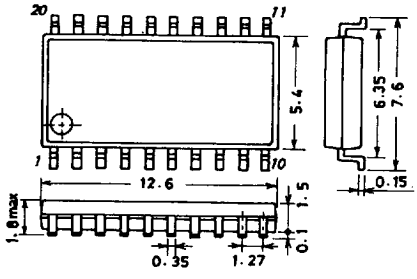
			unit
Maximum Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	−30 to +75	°C
Storage Temperature	Tstg	−40 to +125	°C

Case Outline 3021B
(unit : mm) [LC7881]



SANYO: DIP20Slim

Case Outline 3036B
(unit : mm) [LC7881M]



SANYO: MFP20

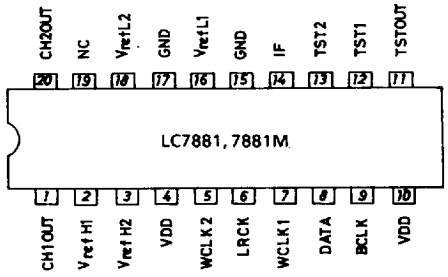
Recommended Operating Conditions		min	typ	max	unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
"H"-Level Reference Voltage	V_{refH}	$V_{DD}-0.5$		V_{DD}	V
"L"-Level Reference Voltage	V_{refL}	0		0.5	V
"H"-Level Input Voltage	V_{IH}	2.2		$V_{DD}+0.3$	V
"L"-Level Input Voltage	V_{IL}	−0.3		0.8	V
Operating Temperature	Topg	−30		75	°C

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0V, unless otherwise specified			min	typ	max	unit
Resolution	RES			16		bits
Conversion Rate	Fs				176.4	kHz
Total Harmonic Distortion	THD1	1kHz, level : 0dB			0.05*1	%
		1kHz, level : 0dB			0.08	%
Crosstalk	C·T	1kHz, level : 0dB		−85		dB
Signal to Noise Ratio	S/N			92		dB
Power Dissipation	Pd			20	40	mW

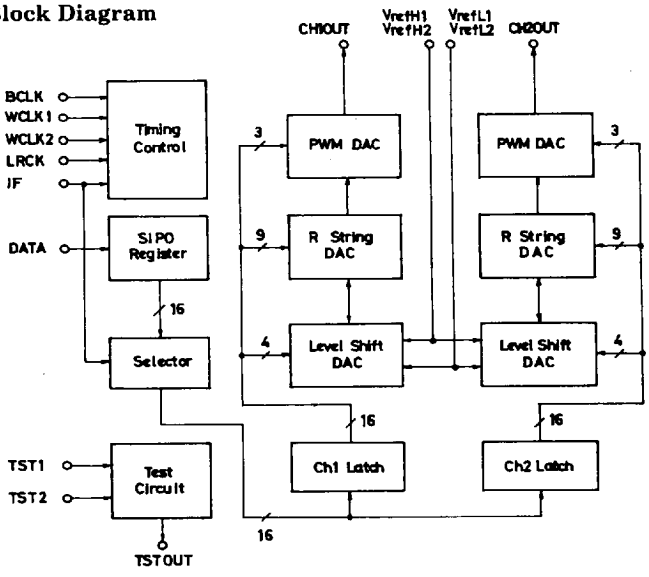
*1 Sorted-out product

Test Circuit : See Sample Application Circuit (1). Sampling frequency Fs = 176.4kHz

Pin Assignment



Equivalent Circuit Block Diagram

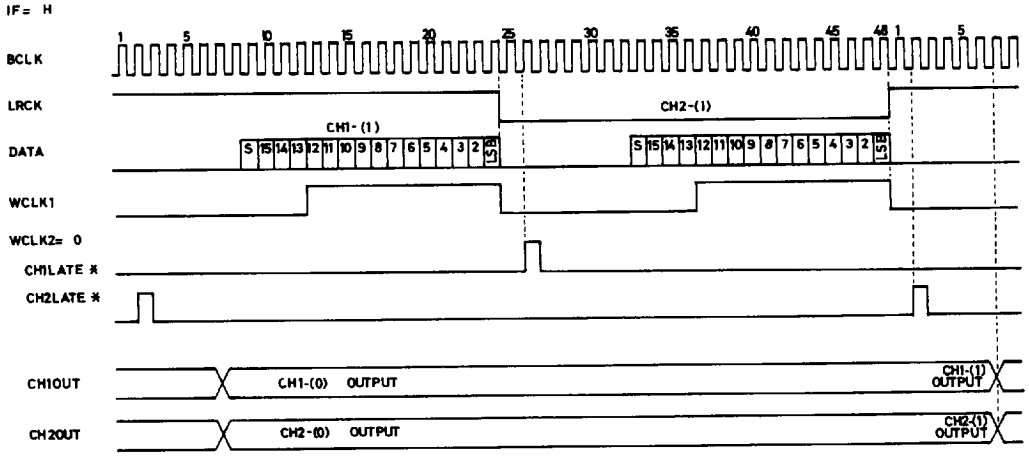


Pin Description

Pin No.	Name	Description
1	CH1 OUT	CH1 output pin
2	VrefH1	Reference voltage "H" input pin 1 (Refer to Operation Description.)
3	VrefH2	Reference voltage "H" input pin 2 (Refer to Operation Description.)
4	V_{DD}	+5V power supply voltage
5	WCLK2	Word clock input #2. When IF is "H" level, WCLK2 must be "L" level. When IF is "L" level and WCLK2 goes LOW, an internal signal is generated that latches the data on the left digital audio channel.
6	LRCK	Left-right clock input. When "H" level, shows that the digital audio input is on the left-channel; when "L" level, on the right-channel.
7	WCLK1	Word clock input #1. When IF is "H" level and WCLK1 goes "L" level, an internal signal is generated that latches the data on both the right and left digital audio channels. When IF is "L" level and WCLK1 goes "L" level, an internal signal is generated that latches the data on the right digital audio channel.
8	DATA	Digital audio data input. When IF is "H" level, data is input in bit-serial format from the most significant bit (MSB). When IF is "L" level, data is input in bit-serial format from the least significant bit (LSB).
9	BCLK	Bit clock input pin. Bit clock for reading in digital audio data in bit-serial format and the clock for the PWM DAC.
10	V_{DD}	+5V power supply voltage
11	TST OUT	Test output, normally open.
12	TST1	Test input, normally ground.
13	TST2	Test input, normally ground.
14	IF	Interface toggle. Digital audio data is input MSB first when "H" level, and LSB when "L" level.
15	GND	Ground
16	VrefL1	Reference voltage "L" level input (Refer to Operation Description.)
17	GND	Ground
18	VrefL2	Reference voltage "L" level input (Refer to Operation Description.)
19	NC	No connection
20	CH2 OUT	CH2 output pin

SANYO SEMICONDUCTOR CORP

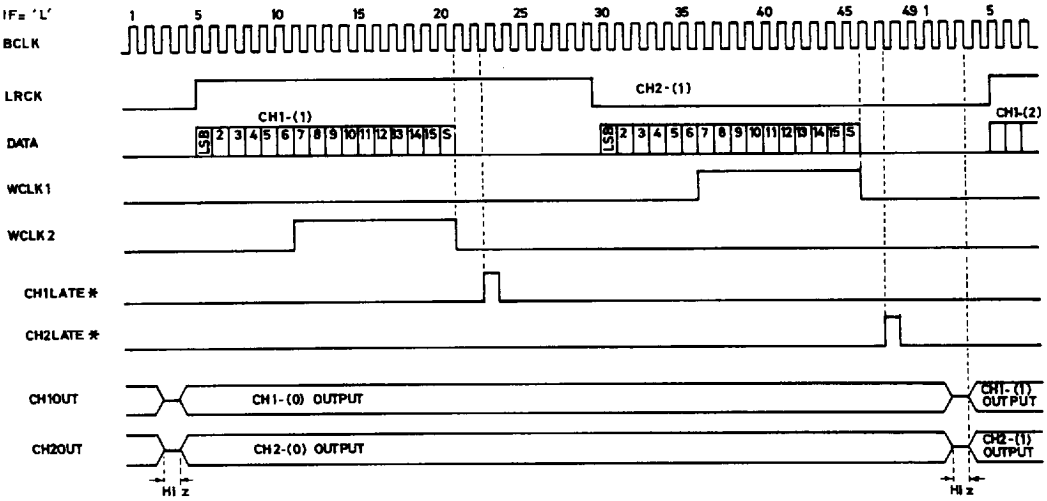
Timing Chart 1



* CH1LATE, CH2LATE : Internal signal

BCLK= 8.4672 MHz (Fs=176.4 kHz)
= 4.2336 MHz (Fs= 88.2 kHz)
= 2.1168 MHz (Fs= 44.1 kHz)

Timing Chart 2



* CH1LATE, CH2LATE : Internal signal

BCLK= 8.6436 MHz (Fs=176.4 kHz)
4.3218 MHz (Fs= 88.2 kHz)
2.1609 MHz (Fs= 44.1 kHz)

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Operation Description

(1) Reading In Digital Audio Data

Digital audio data is a 16-bit serial signal in 2's complement format. The LC7881 supports two digital audio data formats - - - LSB first and MSB first, depending on the level of the IF pin. The data input at the DATA pin is input to the CH1 latch, CH2 latch of the two D/A converters built in CH1, CH2 by time sharing.

① MSB first (IF = "H" level) See Timing Chart 1.

The digital data is written from the DATA terminal to the SIPO register in sync with BCLK rise, starting from the MSB. (Data changes on the negative transition of BCLK.)
The CH1 latch enable (CH1LATE) signal and CH2 latch enable (CH2LATE) signal cause the CH1 data and CH2 data to be latched into the CH1 Latch and CH2 Latch, respectively.
Work clock 1 (WCLK1) fall must align with digital data (DATA) end.
When CH1LATE is "H" level, LRCK must be "L" level and when CH2LATE is "H" level, LRCK must be "H" level. (See Timing Chart 1 · · · · · CH1LATE, CH2LATE.)

② LSB first (IF = "L" level) See Timing Chart 2.

The digital data is written from the DATA terminal to the SIPO register in sync with BCLK fall, starting from the LSB. (Data changes on the positive transition of BCLK.)
The CH1 latch enable (CH1LATE) signal and CH2 latch enable (CH2LATE) signal cause the CH1 data and CH2 data to be latched into the CH1 Latch and CH2 Latch, respectively.
Word clock 1 (WCLK1) fall, word clock 2 (WCLK2) fall must align with digital data (DATA) end.
When CH1LATE is "H" level, LRCK must be "H" level and when CH2LATE is "H" level, LRCK must be "L" level. (See Timing Chart 2 · · · · · CH1LATE, CH2LATE.)

(2) Conversion (See Fig.1.)

The LC7881 has two, independent on-chip D/A converters for the CH1 and CH2. Both use dynamic level shift, combining resistance strings, pulse-width modulation and level shift D/A conversion modes.
The digital audio data for the right and left channels, which is input from the DATA pin using time-division multiplexing, is converted and output in-phase from the CH1OUT and CH2OUT pins.
Specially, the 16-bit digital audio data signal (D_{15} to D_0) is latched, then :

I the 9 MSBs (D_{15} to D_7) go to the R-string DAC;
II the 3 intermediate bits (D_6 to D_4) go to the PWM BAC, and;
III the 4 LSBs (D_3 to D_0) go to the level-shift DAC.

The digital audio data in the CH1, CH2 that is input at the DATA pin by time sharing is D/A-converted, and then output in-phase to the CH1OUT pin, CH2OUT pin.

① R-string DAC

This 9-bit circuit has 512 ($=2^9$) unit resistors (R) connected in series so that a potential applied to both ends is subjected to 512-way division.
The two adjoining potentials V2 and V1 of the divided potentials corresponding to the value of the 9 MSBs of data (D_{15} to D_7) are sent via a switching circuit to the PWM DAC.
At this point, $V2 - V1 = (V_H - V_L)/512$

② PWM DAC

This is a 3-bit circuit that applies pulse width modulation to voltages V2 and V1 output from the R-string DAC to produce an 8-way division.
Depending on the value of the data in bits D_6 to D_4, one of the voltages, V2 or V1, is output to the CH1OUT (or CH2OUT) pin.
The PWM clock uses BCLK, with values depending on the conversion and BCLK frequencies as shown in Table 1 next page.

Table 1 Conversion and BCLK Frequencies

IF pin	Conversion Frequency	BCLK Frequency
"H" level	44.1kHz	2.1168MHz
	88.2kHz	4.2336MHz
	176.4kHz	8.4672MHz
"L" level	44.1kHz	2.1609MHz
	88.2kHz	4.3218MHz
	176.4kHz	8.6436MHz

Note 1 : PWM performs 3 cycles in each conversion cycle.
Note 2 : When the IF pin is "L" level, 1 clock cycle during the conversion period is Hi-z.

③ Level shift DAC

The variable resistors VRH and VRL are connected in series to the two ends of the R-string converter resistance, configuring a 4-bit D/A conversion circuit. Depending on the values of the data in the LSBs (bits D_3 to D_0), VRH and VRL change as follows:

1) The sum of VRH and VRL is constant, irrespective of the data value.
2) VRH and VRL are in the range of 0 to 15R/128 (where R is the unit resistance of the R-string converter) and resistance changes in R/128 steps in accordance with the data value. This means that the R-string converter outputs, V2 and V1, vary in the range of 0 to $15 \times \Delta V/128$ (where $\Delta V = (V_H - V_L)/512$), in $\Delta V/128$ steps.

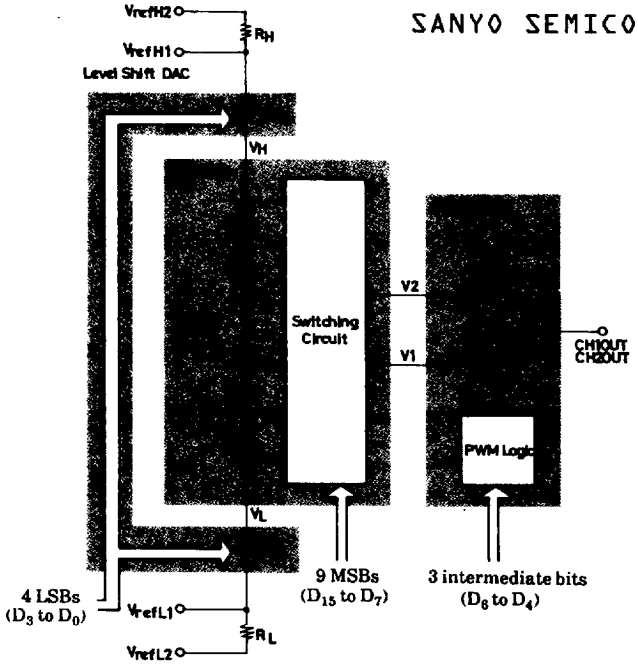


Fig.1 D/A Conversion System of the LC7881

(3) Vref Terminal (See Fig.1.)

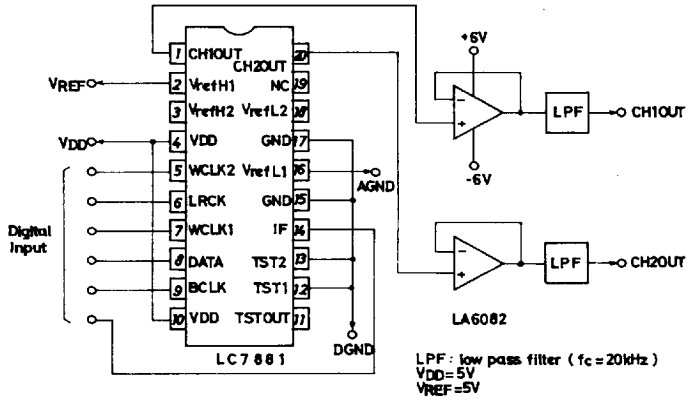
The voltage on Vref terminal used to apply the reference voltage to the resistance strings is normally such that VrefH1 = 5V, VrefL1 = 0V (with VrefH2, VrefL2 open).

When the output amplitude is made small to obtain matching to the input amplitude of the operational amplifiers connected to the LC7881 output pins, VrefH2 and VrefL2 are set to 5V and 0V, respectively. (Connect a capacitor of approximately 100μF across VrefH1 and GND and across VrefL1 and GND.)

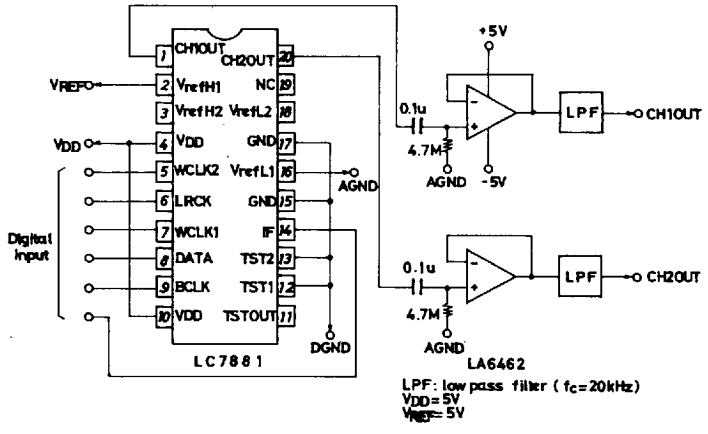
In this case, the on-chip RH, RL cause the maximum output amplitude of the LC7881 (at 0dB playback mode) to be in the range of 1.5V to 3.5V (2Vp-p). See Sample Application Circuits (3).

Sample Application Circuits

(1)



(2) C Cut of Output



(3) Single 5V Power Supply

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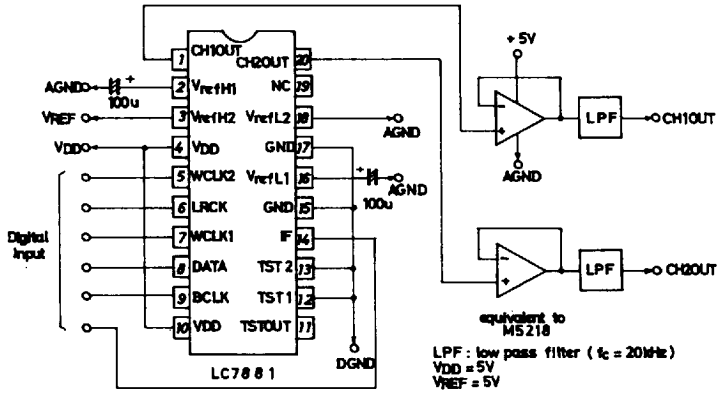

The internal resistors (RH and RL shown in Fig.1) limit the maximum amplitude to about 2V (peak to peak) level.

Notes :

① DGND and AGND shown in Sample Application Circuits must be connected to GND of digital circuit and analog circuit, respectively.

② For V_{DD}, Vref, a low impedance, high stability power supply (commercially available 3-terminal regulator or its equivalent) should be used.

③ Pins 1 and 20, whose output impedance is high (several kΩ), are liable to be affected by noise, requiring noise prevention circuitry such as shortening of wiring between pin and operational amplifier. The two buffer OP AMPs should have the voltage-follower circuit configuration.

④ The CMOS latch-up might be caused due to the to the different power-on timings of pins 4 and 10 (V_{DD}). To prevent such a timing error, power should be applied to these pins from the same power source.