TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT

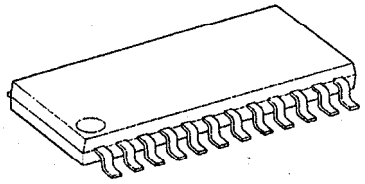
TC9404F, TC9404FN

SILICON MONOLITHIC

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH ANALOG FILTER

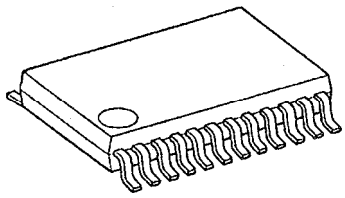
TC9404F, TC9404FN are a 2'nd order Σ-Δ modulation system 1bit DA converter with a built-in 8 times over sampling digital filter and analog filter developing for digital audio equipment. As this IC is small package, SSOP24 (1.00mm, 0.65mm) and the analog filter has been incorporated, it is able to output a direct analog wave form and construct small the digital filter~the analog output unit at a low price.

TC9404F



SSOP24-P-300

TC9404FN



SSOP24-P-300A

Weight SSOP24-P-300 : 0.31g (Typ.)
SSOP24-P-300A : 0.14g (Typ.)

FEATURES

- Built in 8 times over sampling digital filter
- Low voltage operate (3.0V)
- Built-in digital de-emphasis filter (32kHz, 44.1kHz, 48kHz)
- Permits microcontrollers to attenuate output levels (128steps) during serial control mode
- It is possible to do soft mute output level during parallel control mode (64step, 20ms)
- Over sampling ratio (OSR) of Σ-Δ modulation circuit is 192fs
- Built-in digital 0 detection
- Compatible with double speed operation
- Built-in 3'rd order analog filter
- Characteristics of the digital filter and DA converter are as follows :

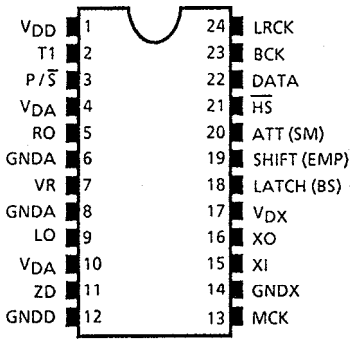
DIGITAL FILTER (fs = 44.1kHz)

	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP BAND SUPPRESSION
Standard Operation	8fs	±0.11dB	20k~24.1kHz	−26dB
Double Speed Operation	8fs	±0.11dB	20k~24.1kHz	−26dB

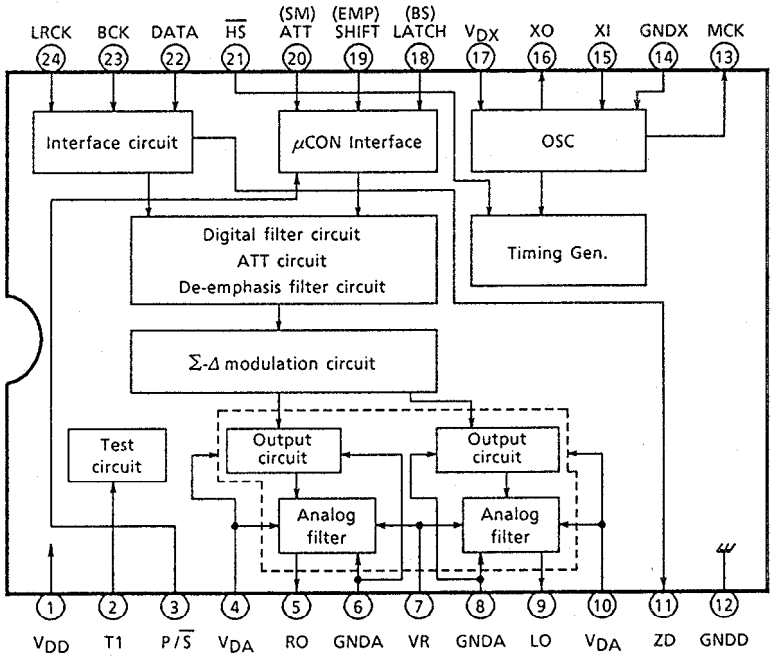
DA CONVERTER (V_{DD} = 5V)

	OSR	NOISE DISTORTION	S/N
Standard Operation	192fs	−85dB (Typ.)	96dB (Typ.)
Double Speed Operation	96fs	−85dB (Typ.)	86dB (Typ.)

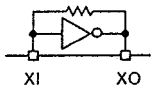
PIN CONNECTION



BLOCK DIAGRAM



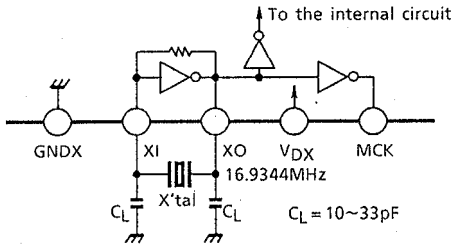
PIN FUNCTION

PIN No.	SYMBOL	I/O	FUNCTION	REMARKS
1	V_{DD}	—	Logic power supply terminal.	
2	T1	I	Test terminal. Normally, use at "L".	
3	P/$\overline{S}$	I	Parallel control, serial control switching terminal.	
4	V_{DA}	—	Analog power supply terminal.	
5	RO	O	R-ch analog output terminal.	
6	GNDA	—	Analog ground terminal.	
7	VR	I	Reference voltage input terminal.	
8	GNDA	—	Analog ground terminal.	
9	LO	O	L-ch analog output terminal.	
10	V_{DA}	—	Analog power supply.	
11	ZD	O	Digital 0 detection output terminal.	
12	GNDD	—	Digital ground terminal.	
13	MCK	O	Master clock output terminal.	
14	GNDX	—	Crystal oscillator ground terminal.	
15	XI	I	Crystal oscillator connection terminal. Connect to a crystal oscillator, generates needed frequency for the system.	
16	XO	O		
17	V_{DX}	—	Crystal oscillator power supply terminal.	
18	LATCH (BS)	I	Serial control : Data latch signal input terminal for ATT Parallel control : De-emphasis filter mode select terminal.	SHUMITT INPUT
19	SHIFT (EMP)	I	Serial control : Shift clock input terminal for ATT Parallel control : De-emphasis filter control terminal.	SHUMITT INPUT
20	ATT (SM)	I	Serial control : Data input terminal for ATT Parallel control : Soft mute control terminal.	SHUMITT INPUT
21	$\overline{HS}$	I	Standard/double speed operation mode switching terminal. Standard operation at "H", double speed operation at "L".	
22	DATA	I	Data input terminal.	
23	BCK	I	Bit clock input terminal.	
24	LRCK	I	LR clock input terminal.	

DESCRIPTION OF BLOCK OPERATION

1. Crystal oscillation circuit and timing generator

Clock required for internal operation can be generated when crystal and capacitors are connected as shown in the following figure.
Further, this converter is also operable when system clock is input from the outside through XI terminal pin⑮.
However, a through consideration is required in this case because noise distortion and S/N ratio of the DA converter are largely affected by qualities of wave form such as jitter, rise and fall characteristics, etc. of system clock.



Use a crystal having a low CI value and good statability.

Fig.1 Configuration of crystal oscillation circuit.

The timing generator generates clock required for the digital filter, de-emphasis filter, interpolation filter and process timing signal.

2. Data input circuit

DATA and LRCK are taken in the shift register in the LSI at the rise edge of BCK.
As shown in the following timing example, it is therefore necessary to input DATA and LRCK in synchronism with the fall edge of BCK.
Further, because DATA has been to designed that 16 bits before the change point of LRCK are made effective data.

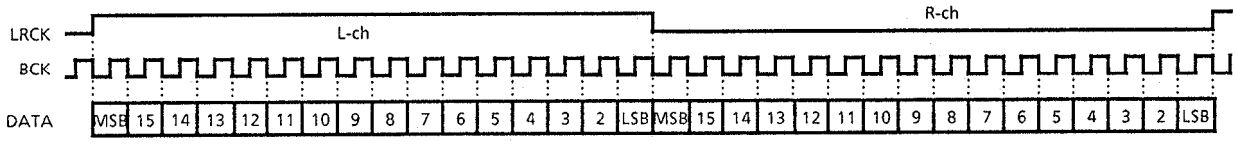


Fig.2a Example of input timing diagram

3. Digital filter

Foldover noise component outside the band is removed by the 8 times oversampling digital filter.

Table-1 Characteristics of the digital filter

	PASS-BAND RIPPLE	TRANSIENT BANDWIDTH	STOP-BAND SUPPRESSION
Standard operation	±0.011dB	20.0k~24.1kHz	−26dB
Double speed operation	±0.011dB	20.0k~24.1kHz	−26dB

Frequency characteristics of the digital filter are as follows : (Double speed operation is same)

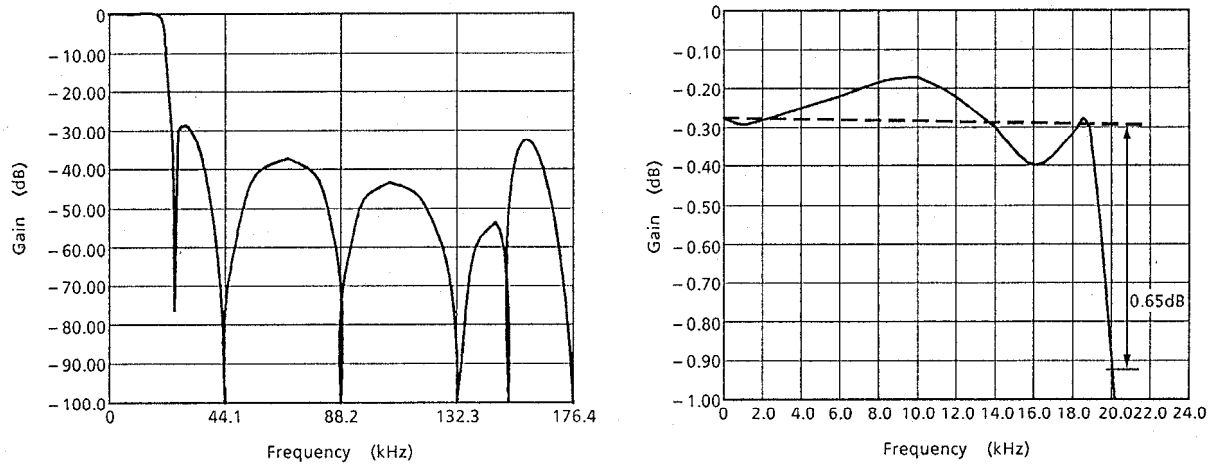


Fig.3 Digital filter frequency characteristics (fs = 44.1kHz)

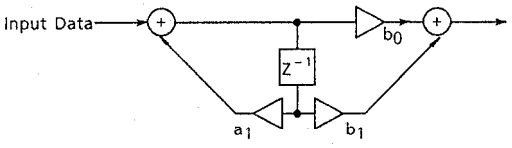
4. De-emphasis filter

The built-in digital de-emphasis circuit is capable of setting sampling frequency, fs, of 32kHz, 44.1kHz, and 48kHz. The selection is done as shown in the following table.

Table-2 Truth table for de-emphasis filter selection

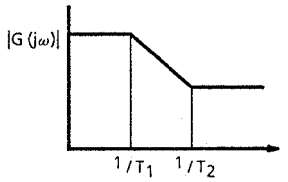
LATCH (BS)	H	H	L	L	
SHIFT (EMP)	H	L	H	L	
MODE (fs SELECT)	32	48	44.1	OFF	(kHz)

Digitization of the de-emphasis filter has eliminated the necessity for external parts such as resistor, capacitor, analog switch, etc.
Further, to reduce the characteristic error of the de-emphasis filter, coefficients have been adjusted. The construction and characteristics of the de-emphasis filter are shown below.



Transfer function : $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Fig.4 Construction of IIR type digital de-emphasis filter

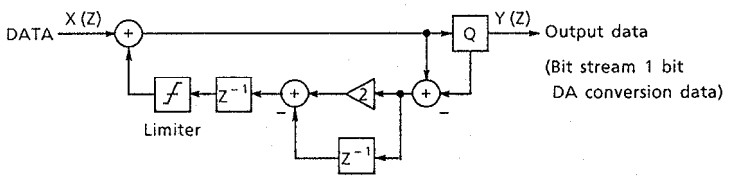


$T_1 = 50\mu s$, $T_2 = 15\mu s$

Fig.5 Filter characteristic

5. DA conversion circuit

The 2'nd order Σ-Δ modulation system DA converter for 2 channels (simultaneous output type) has been incorporated.



2'nd order Σ-Δ modulator : $Y(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z)$

Fig.6 Construction of Σ-Δ modulation DA converter

It has been designed that clock for the Σ-Δ modulator is a half of master clock (MCK : Crystal oscillation clock) and the converter operates at 192fs at the standard operation.
The noise shaping characteristic is shown below.

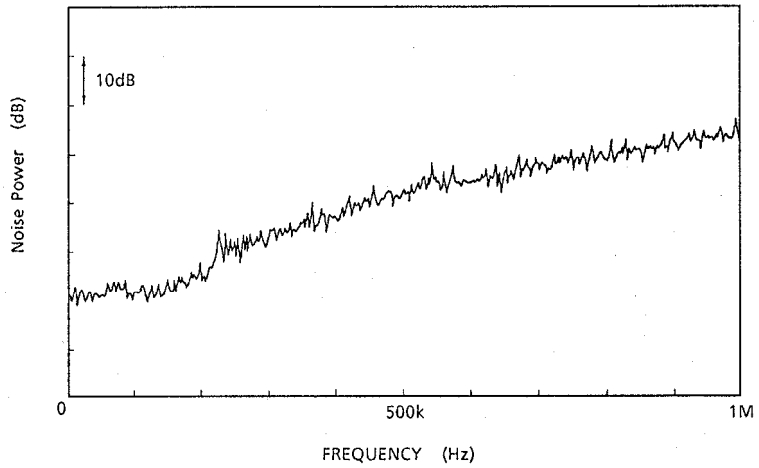


Fig.7 Noise shaping characteristic

6. Output circuit

These ICs is a built-in 3'rd order analog low pass filter.
These output is analog signal directly, RO (pin⑤) and LO (pin⑨) terminal.

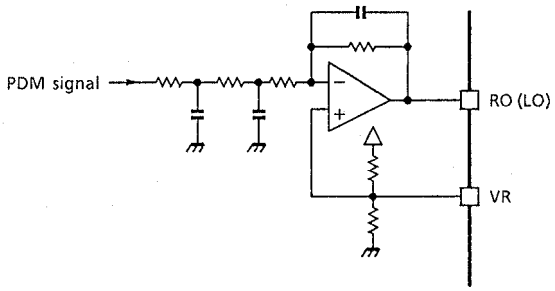


Fig.8 Analog filter circuit

7. Soft mute circuit

This IC is a built-in soft mute circuit, it is possible to do soft mute, when SM terminal is changed "L" level to "H" level during parallel mode.
Characteristic of soft mute ON/OFF and DA converter output level is as follows.
While output level is changing, it is not possible to accept soft mute ON/OFF control.

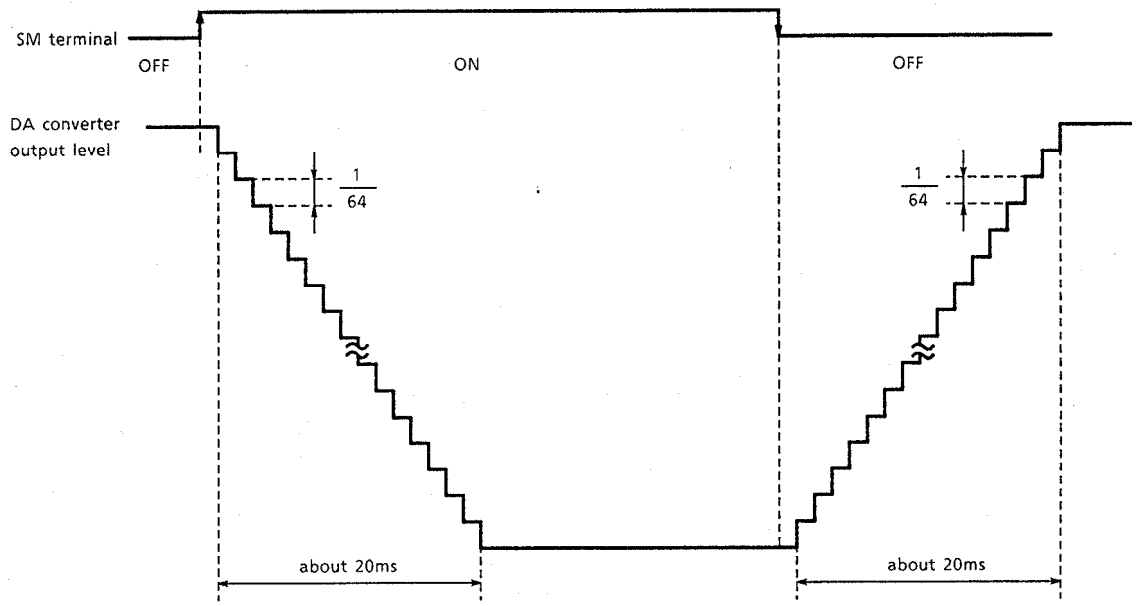


Fig.9 Soft mute DA converter output level

8. These ICs have a built-in input data digital zero detection function.
If zero data is continued for over about 350ms, ZD terminal is changed "L" level to "H" level.

9. Internal control signal explanation

Parallel and serial control mode can be selected by the P/$\overline{S}$ terminal. The controll functions are example as follow.

9-1 Parallel control mode (P/$\overline{S}$ terminal = H)

In parallel control mode, pin⑱, ⑲, ⑳ are set as follows.

Table-3 Terminal name at parallel mode

PIN No.	PIN NAME	FUNCTION
18	BS	De-emphasis filter mode select terminal
19	EMP	De-emphasis filter control terminal
20	SM	Soft mute control terminal.

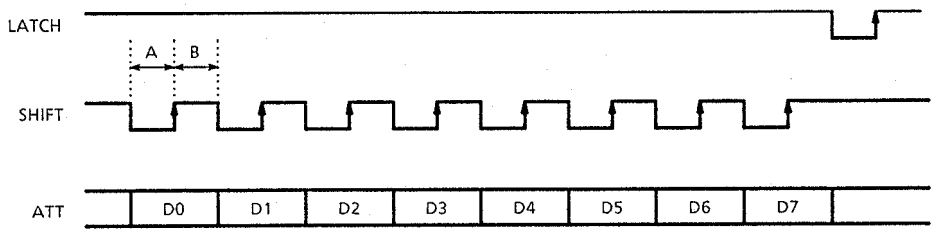
9-2 Serial control mode (P/$\overline{S}$ terminal = L : For micro processor control use)

In serial control mode, these ICs can be controlled by micro processor. The control function of pin⑱, ⑲, ⑳ are as follows.

Table-4 Terminal name at serial mode

PIN No.	PIN NAME	FUNCTION
18	LATCH	Data latch signal input terminal
19	SHIFT	Shift clock signal input terminal
20	ATT	Att data input terminal

LATCH and ATT signal are entered to the shift register of the LSI at the rising edge of SHIFT signal. Also, LATCH signal should rise after a minimum of 1.5μs of the last data is shifted to the register. If the shift pulse is changed while LATCH is Low, Mis-operation may occur. LATCH should be keep at Low until after D7 is shifted into the register.



A = more 1.5μs B = more 1.5μs

Fig.10 Example for serial control mode data

In serial control mode, the control features are as follows.
When this IC's power is ON, all these data must be setting.

Table-5 Serial mode control

SERIAL INPUT DATA	CONTROL SIGNAL	
D7	0	1
D6	AT6	μBS
D5	AT5	μEMP
D4	AT4	—
D3	AT3	—
D2	AT2	—
D1	AT1	—
D0	AT0	—

AT0~6 : Attenuation level setting
μBS : De-emphasis mode select
μEMP : De-emphasis ON / OF

① Digital attenuator

D7 = L is the command for digital attenuator. It can be set to 128 levels as show below.

Table-6 Audio output of attenuation data

ATTENUATION CONTROL DATA D6~D0	AUDIO OUTPUT
7F (HEX)	0dB
7E (HEX)	−0.13dB
⋮	⋮
01 (HEX)	−42.144dB
00 (HEX)	−∞

The attenuation value can be calculated from input data as follow :

ATT = 20ℓog (input data / 128)dB

Example : In case of attenuator = 7A

ATT = 20ℓog (122 / 128)dB = −0.417dB

D7 = H is the command for Digital De-emphasis filter.

② Digital De-emphasis filter

The digital de-emphasis filter can be controled by μEMP and μBS signal.

Table-7 De-emphasis filter setting

μBS	H	H	L	L
μEMP	H	L	H	L
MODE	32	48	44.1	OFF

(kHz)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~6.0	V
		V_{DA}	−0.3~6.0	
		V_{DX}	−0.3~6.0	
Input Voltage		V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9404F	P_D	200	mW
	TC9404FN		200	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DA} = 5V$)

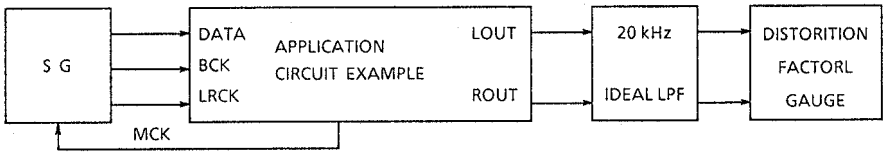
DC item

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Operating Supply Voltage (2)		V_{DD}	—	Ta = −15~55°C (Operation frequency 10MHz ≦ f_{opr} ≦ 17MHz)	2.7	3.0	5.5	V
		V_{DX}			2.7	3.0	5.5	
		V_{DA}			2.7	3.0	5.5	
Power Dissipation		I_{DD}	—	XI = 16.9MHz	—	12	20	mA
Input Voltage	"H" Level	V_{IH}	—		$V_{DD} \times 0.7$	—	V_{DD}	V
	"L" Level	V_{IL}			0	—	$V_{DD} \times 0.3$	
Input Current	"H" Level	I_{IH}	—		−10	—	10	μA
	"L" Level	I_{IL}						

AC item (Over-sampling ratio = 192fs)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Table Harmonic Distortion + Noise 1	THD + N1	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	−85	−80	dB
Table Harmonic Distortion + Noise 2	THD + N2	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	−85	−78	dB
S/N Ratio	S/N	1		88	96	—	dB
Dynamic Range	DR	1	1kHz Sine wave, −60dB input conversion	90	95	—	dB
Cross-talk	CT	1	1kHz Sine wave, full-scale input	—	−95	−90	dB
Analog Output Level 1	Aout 1	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 5V$	—	1250	—	mV_{rms}
Analog Output Level 2	Aout 2	1	1kHz Sine wave, full-scale input $V_{DD} = V_{DX} = V_{DA} = 3.0V$	—	750	—	mV_{rms}
Operating Frequency	f_{opr}	—	$V_{DD} = V_{DA} = V_{DX} \geqq 4.5V$	10	16.9344	19.2	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	2.1168	4.3	MHz
Rise Time	t_r	—	LRCK, BCK (10%~90%)	—	—	15	ns
Fall Time	t_f			—	—	15	ns
Delay Time	t_d	—	BCK ↓ Edge → LRCK, DATA	—	—	40	ns

- **TEST CIRCUIT-1** : Application circuit example is used.

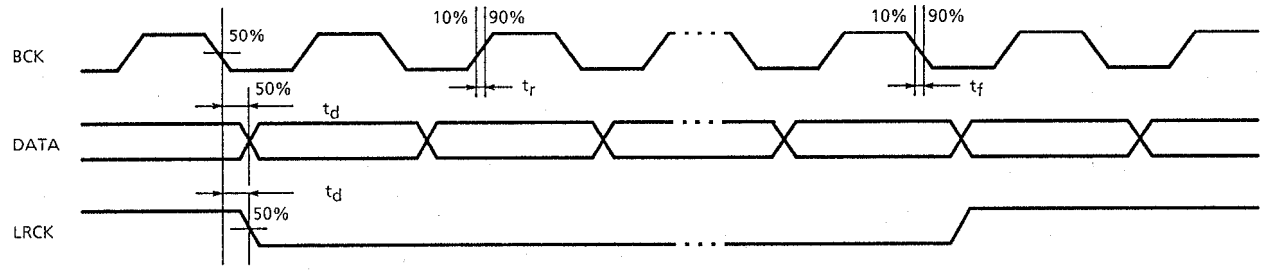


SG : ANRITSU MG-22A or equivalent
LPF : SHIBASOKU 725C built-in Filter
Distortion Factor Gauge : SHIBASOKU 725C or equivalent

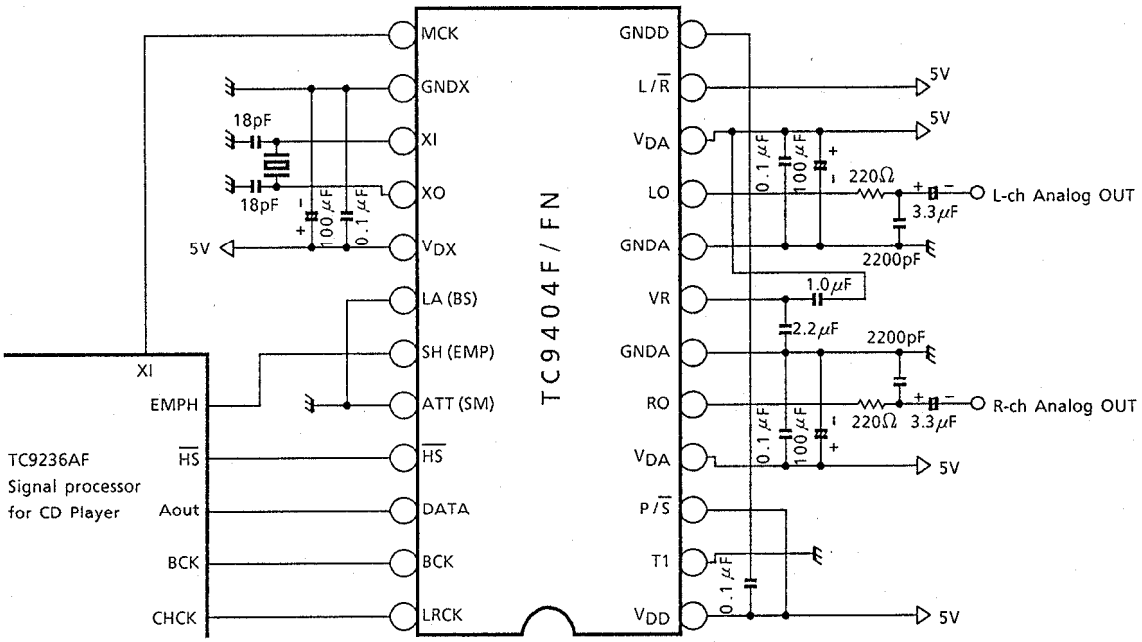
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S / N, DR	ON

A weight : IEC-A or equivalent

- **AC CHARACTERISTIC POINT** (Input signal : LRCK, BCK, DATA)



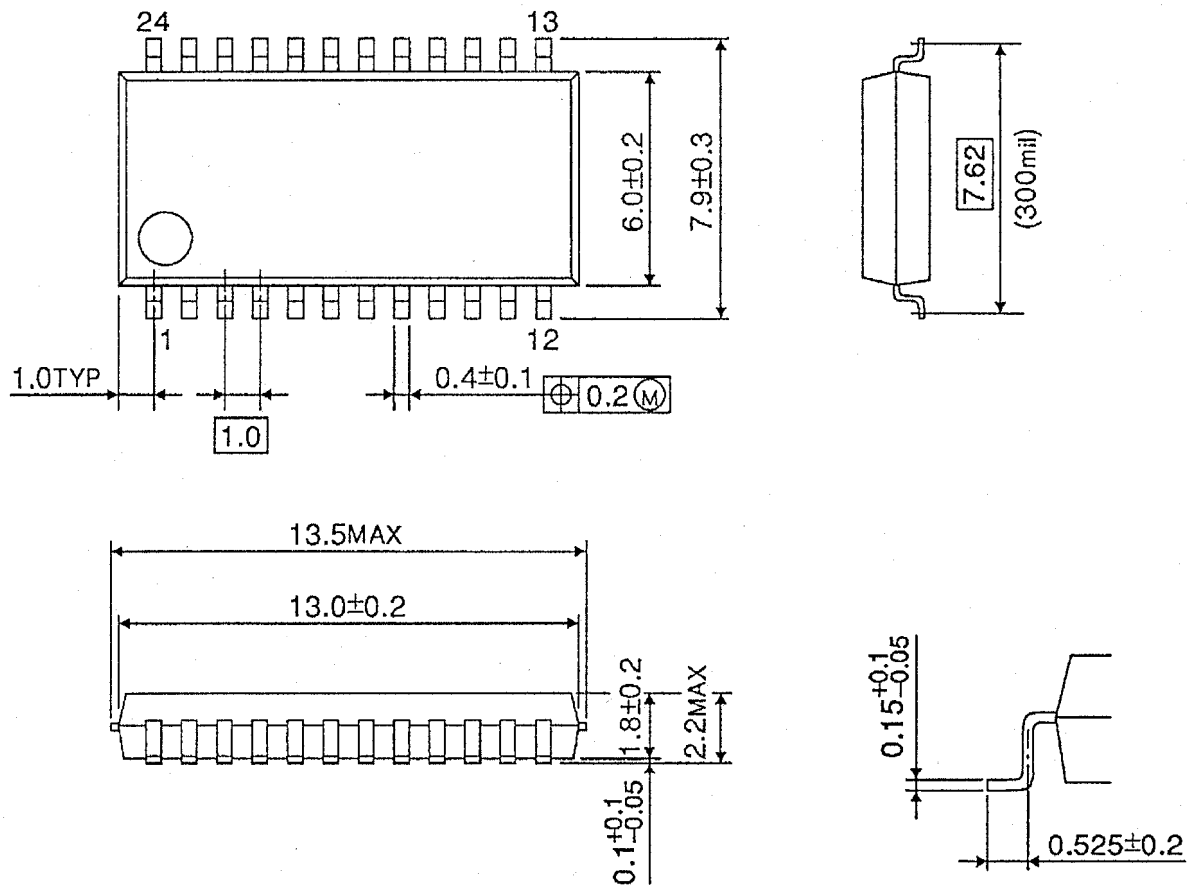
APPLICATION CIRCUIT



OUTLINE DRAWING

SSOP24-P-300

Unit : mm

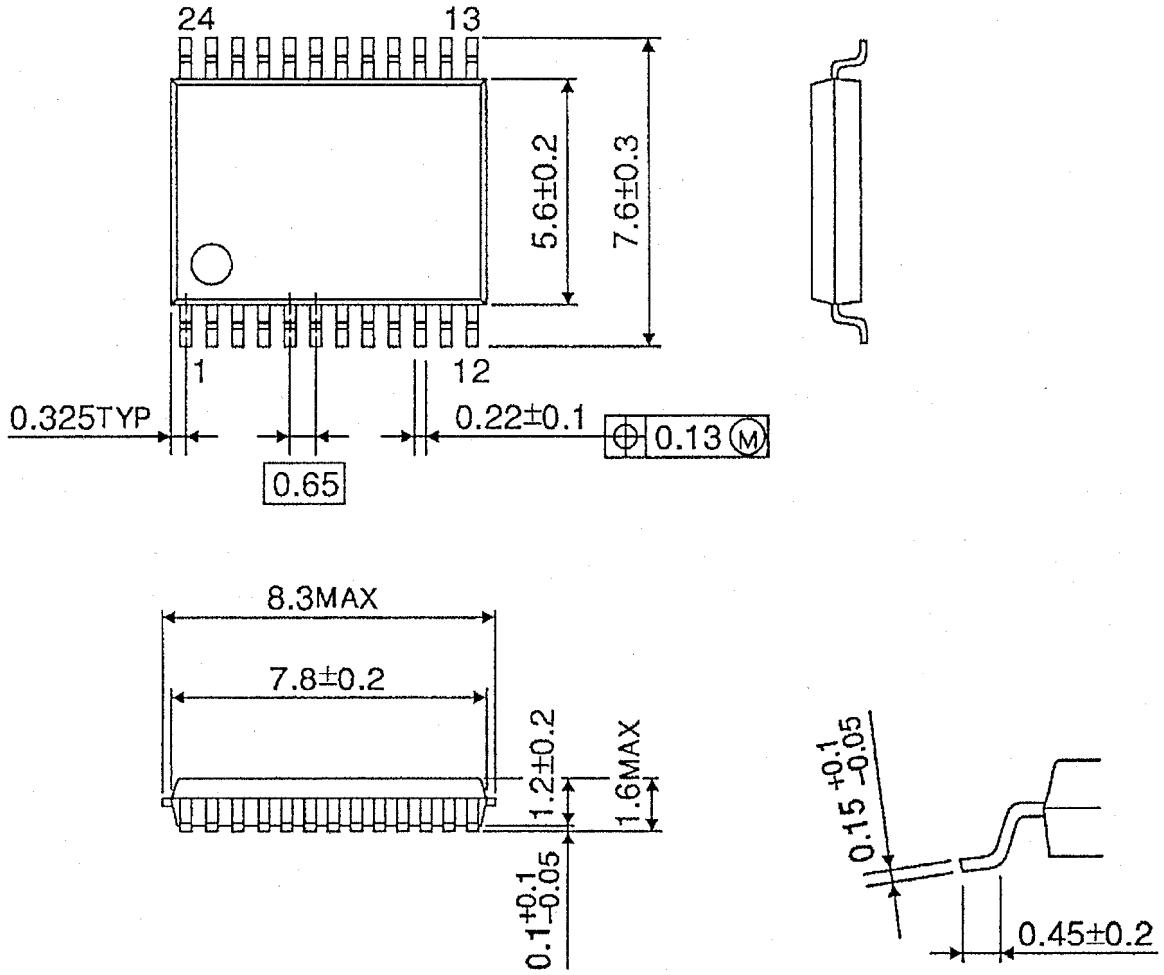


Weight : 0.31g (Typ.)

OUTLINE DRAWING

SSOP24-P-300A

Unit : mm



Weight : 0.14g (Typ.)