PIONEER®
The Art of Entertainment

Service Manual

SERVICE GUIDE

ORDER NO.
RRV1710

DVD PLAYER
DV-500

DVD LD PLAYER
DVL-90
DVL-700

CONTENTS

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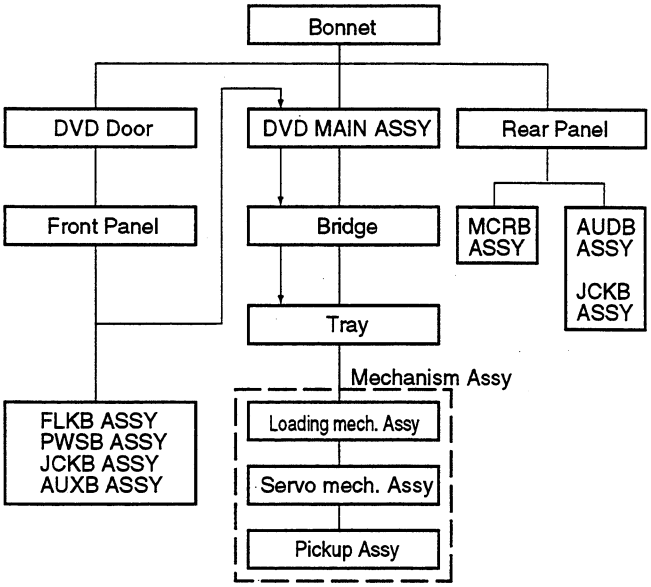
1. DISASSEMBLY

1.1 DV-500

1.1.1 Flow chart



Note : For details, Refer to "7.2 DISASSEMBLY/ASSEMBLY" in the service manual RRV1708 for DV-500.

1.1.2 Manual Setting of the Tray Unit to Its Open Position

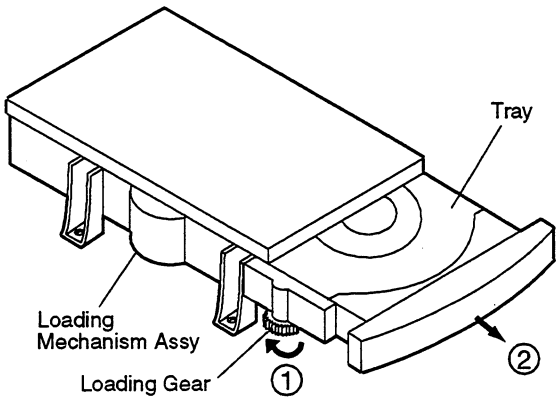
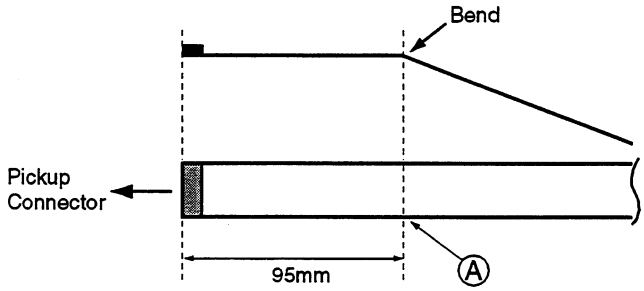


Fig. 1-1

1.1.3 Style the Flexible Cable for Spindle Motor and Pickup

(1) Bend the Pickup Flexible Cable (20P)



(2) Bend the Spindle Motor Flexible Cable (8P)

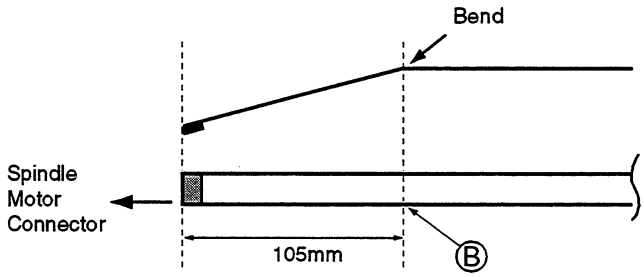


Fig. 1-2-1

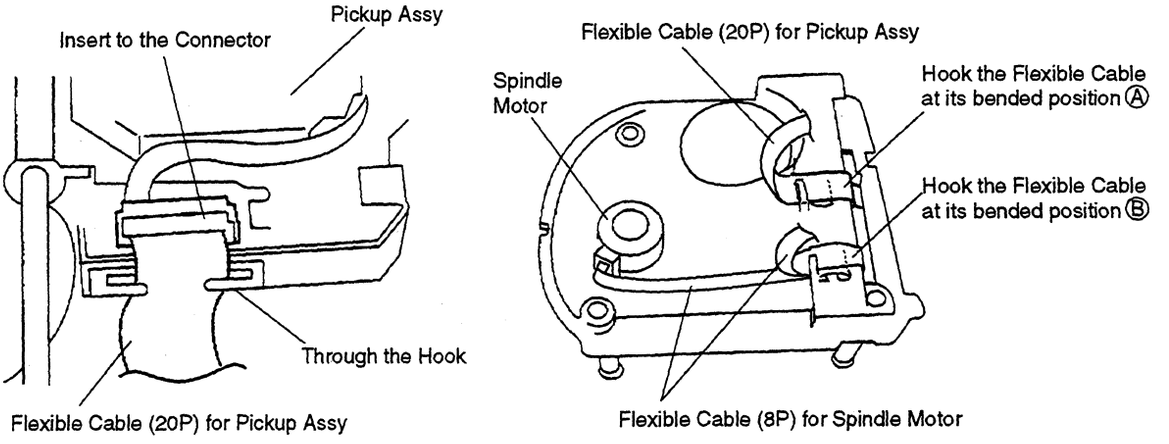


Fig. 1-2-2

1.1.4 Style the Flexible Cable

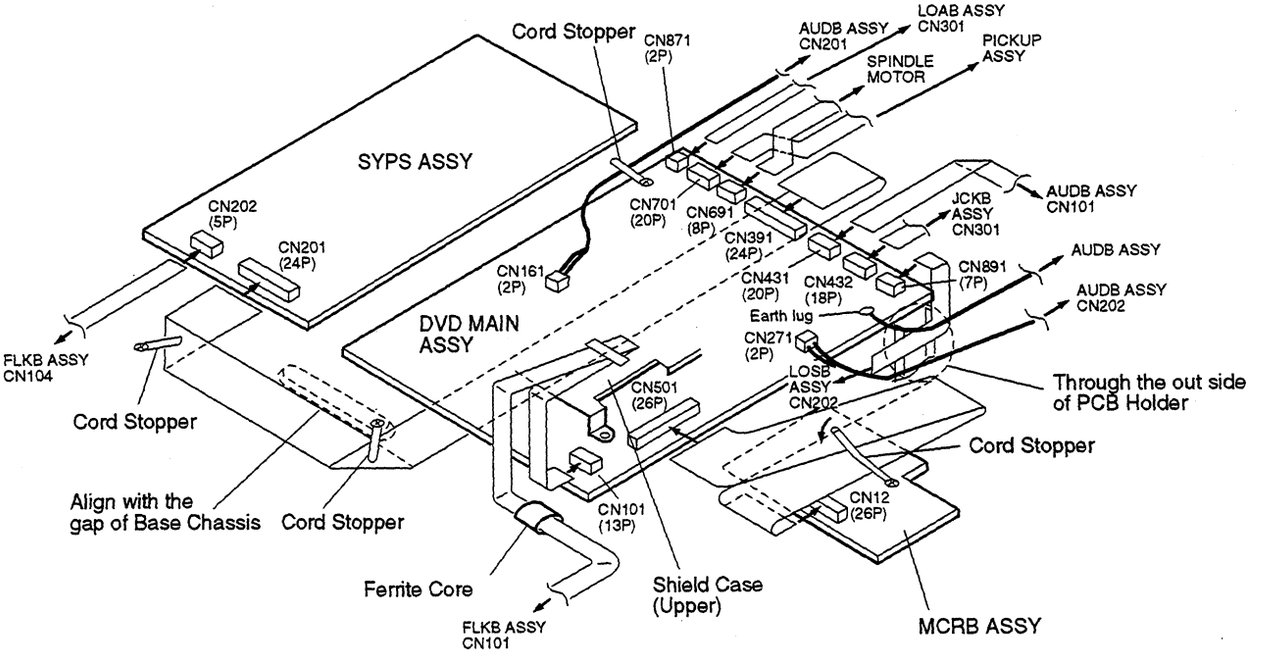


Fig. 1-3

1.2 DVL-90 and DVL-700

1.2.1 Manual Setting of the Tray Unit to Its Open Position

(1) Make sure that the Carriage Assy lens stops at a position outside the broken line indicated in Fig. 1-4.

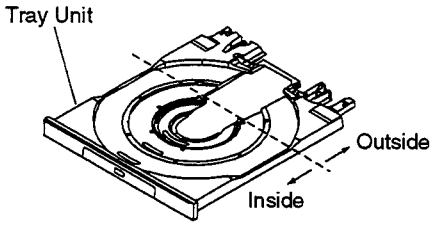


Fig. 1-4

(2) If the lens remains in a position inside the broken line in Fig. 1-4, locate the lens in a position outside the broken line in the following manner: Insert your hand from the lower-left side of the Tray Unit, and turn the Gear Pulley of the Loading Mechanism Unit counterclockwise until it stops so that the Servo Mechanism rises. Then slowly turn the Worm of the Carriage Assy counterclockwise so that the Carriage Assy moves backward and the Carriage Assy lens moves to a position outside the broken line in Fig. 1-4. (Without this procedure, the unit will be in CD Tray Open mode.)

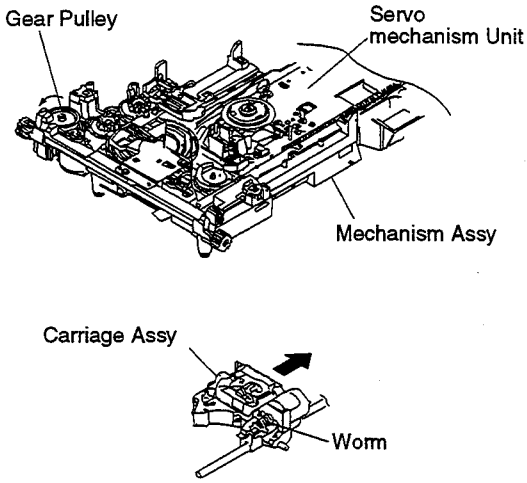


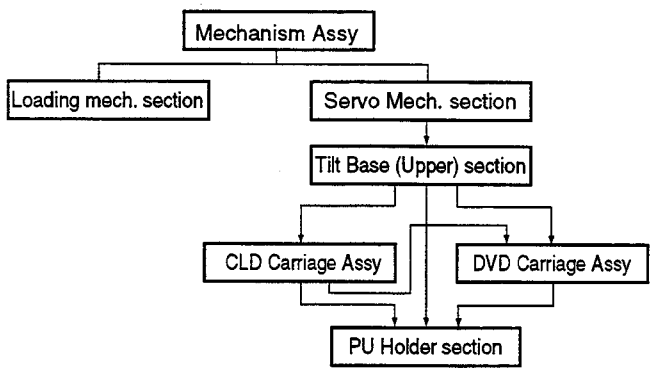
Fig. 1-5

(3) Turn the Gear Pulley of the Loading Mechanism Unit clockwise. When the Servo Mechanism Unit goes down and the Tray Unit moves forward, pull the Tray Unit slowly by hand to its open position.

Note : For removal of the main parts, Refer to "7.2 DISASSEMBLY/ASSEMBLY" in the service manual RRV1709 for DVL-90 and DVL-700.

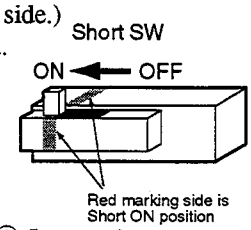
1.2.2 Removal of Mechanism Parts

- **Flowchart of Mechanism Assy Removal**



- **Removal of the Mechanism Assy**

(1) Press the LD OPEN key to remove the Tray Unit. (The Carriage moves to the LD side.)
(2) Disconnect the AC Power Cord.
(3) Set the short-circuit switch of the DVD Carriage Assy so that the position pointer is aligned with the mark (Short-Circuit mode.)



(4) Remove the Clamper section. (① 5 screws)
(5) Remove the Rear Cover. (② 4 screws)
(6) Remove the Tray Stopper that holds the Flexible Cable. (③ 1 screw)

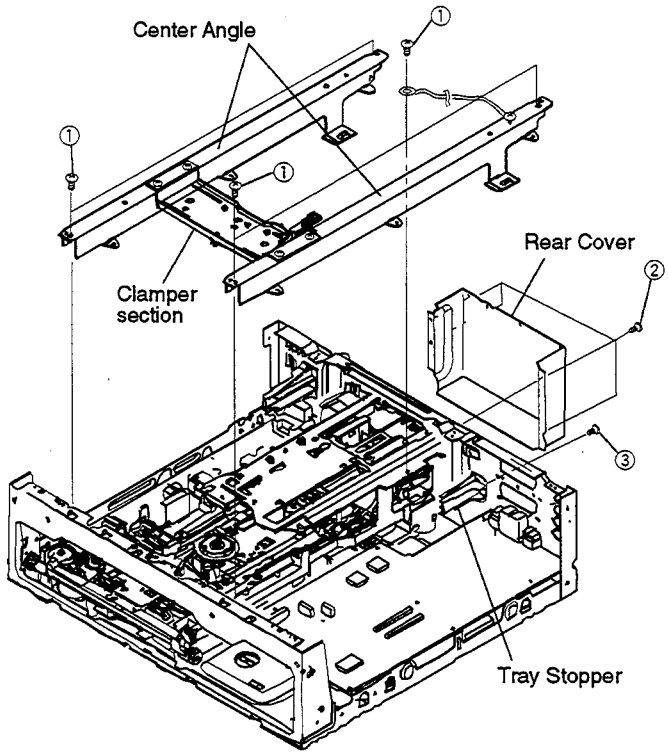


Fig. 1-6

(7) Remove the two Tilt Rear Springs located at the Rear Panel side of the Servo Mechanism section, and hook them onto the provisional hooks Tilt Base (Under).

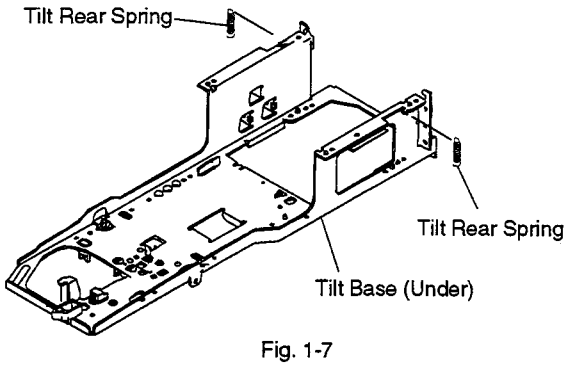


Fig. 1-7

(8) Remove the Cam Holder (L) and Cam Holder (R) located on each side of the Mechanism Assy. (④ 2 screws)
(9) Remove the four mounting screws ⑤ of the Mechanism Assy.

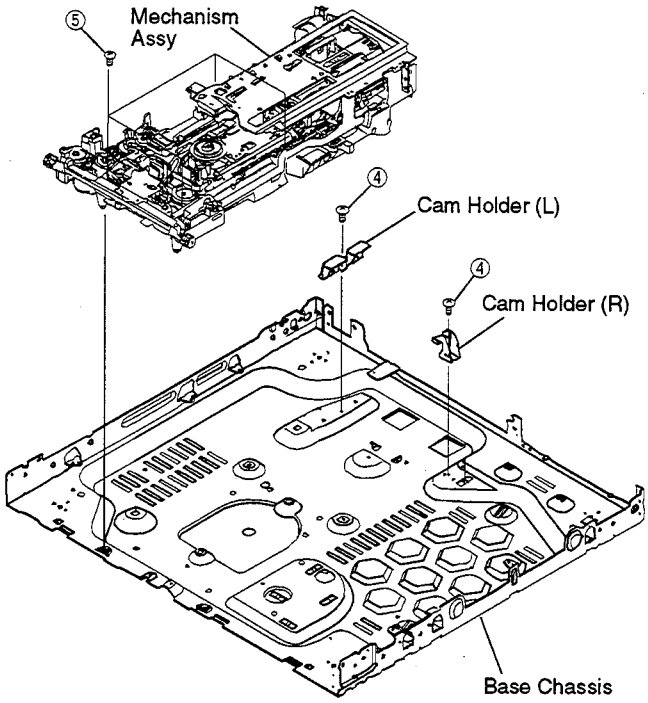


Fig. 1-8

(10) Disconnect the three Flexible Cables connecting the Mechanism Assy and CLD MAIN Assy from CLD MAIN Assy, one Flexible Cable connecting the Mechanism Assy and DVD MAIN Assy from the DVD MAIN Assy, and the Connector Assy (2P) connecting the Mechanism Assy and the POWER SUPPLY Assy from the POWER SUPPLY Assy.
(11) Slide the Mechanism Assy backward while raising it lightly until its front moves to a position where it can be pulled out of the Panel Holder. Then raise the front of the Mechanism Assy and pull it diagonally upward out through the Rear Panel.

• Removal of the Servo Mechanism Section

(1) Remove the Housing Assy (3P/yellow) for FG and the Housing Assy for detection of carriage position (3P/blue) from the LMSB Assy.
(2) Remove the Cam Holder. (⑥ 1 screw)
(3) Remove the CD Plate and the CDP Spring. (⑦ 2 screws)
(4) While pressing the Cam Plate toward the inside (right), turn the Twin Gear counterclockwise until it stops (the Twin Gear and the Cam Gear will become disengaged.)
(5) Bend the hook of Clamp Cam B in the direction indicated by the arrow until it stops.
(6) Remove the Servo Mechanism Unit from the Clamp Cam by raising it directly upward.

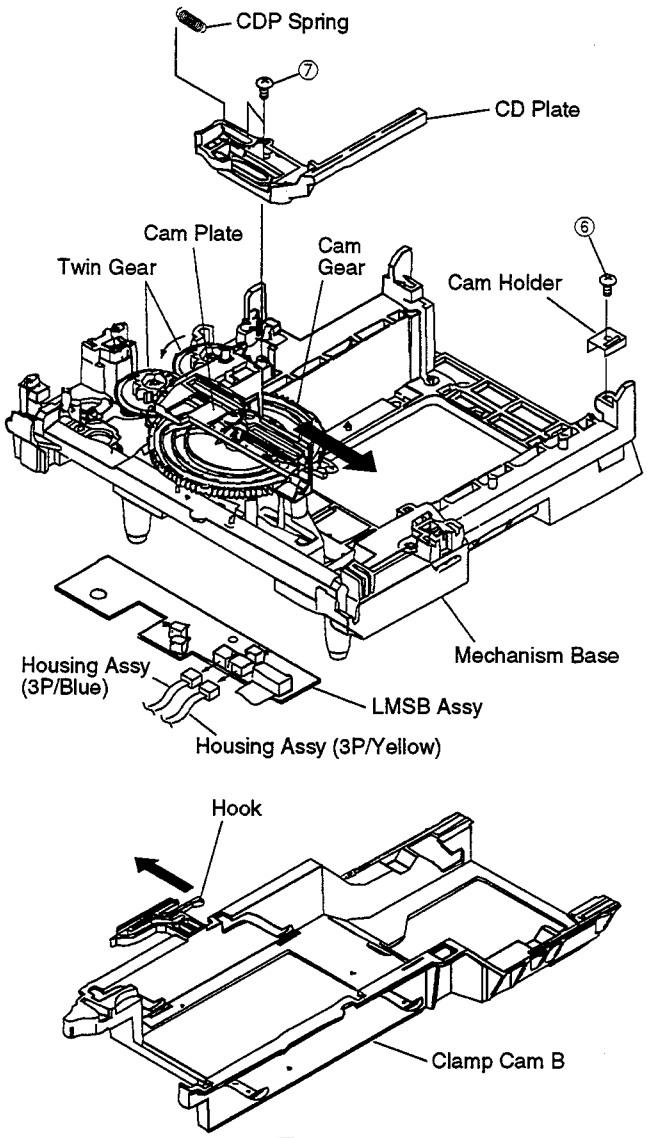


Fig. 1-9

• Removal of the Tilt Base (Upper)

(1) Remove the Shipping Spring and Shipping Lever.
(2) Remove the Housing Assy 2P (blue/white) from the TNMB Assy.
(3) Remove the Tilt Base (Upper). (⑧ 4 screws)

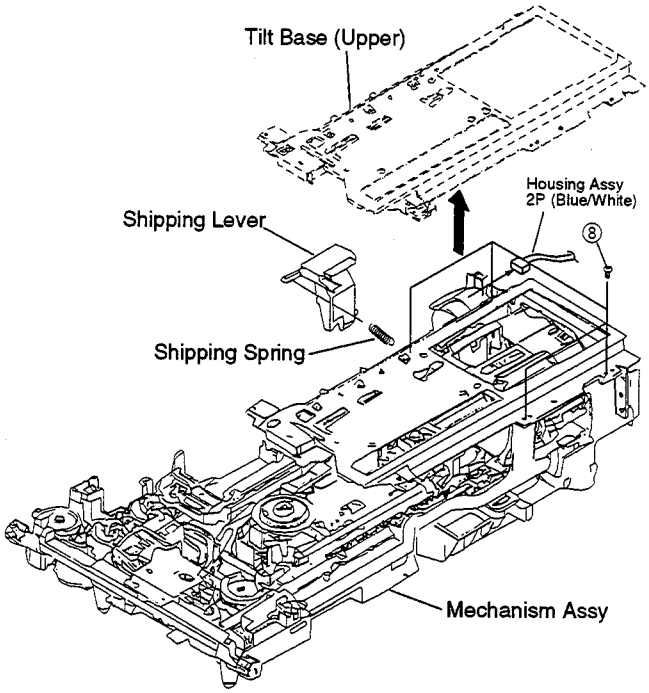


Fig. 1-10

• Removal of the CLD Carriage Assy

(1) Remove FPC Holder B and disconnect the PU flexible cable.
(2) Remove the fixing screw ⑨ of the CA Shaft (Under) and remove it from the CLD Carriage Assy.
(3) Remove the CLD Carriage Assy from the Mechanism Assy.

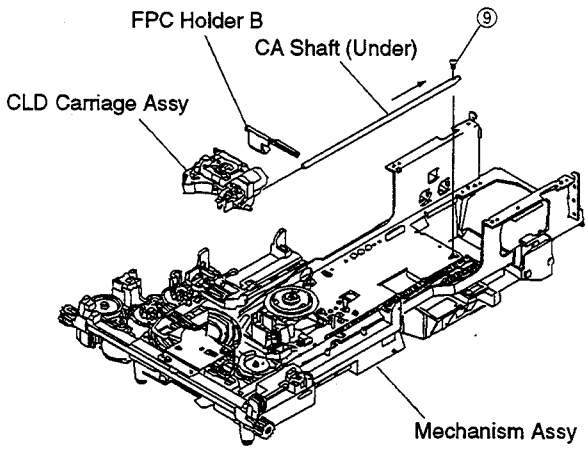


Fig. 1-11

• Removal of the DVD Carriage Assy

(1) Turn the PU Holder 180 degrees by turning the Middle Gear of the Carriage Change Mechanism counterclockwise until it stops.

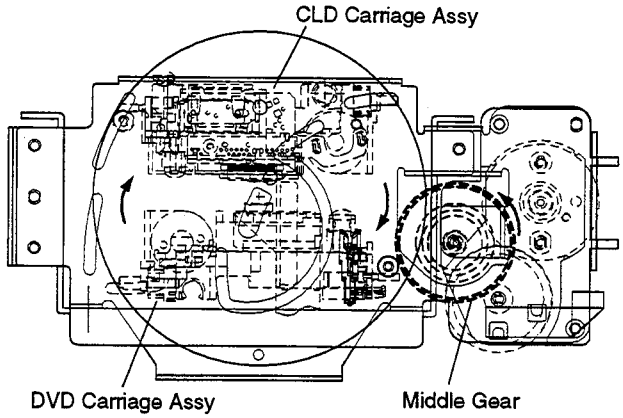


Fig. 1-12 Mechanism Assy (Rear View)

(2) Move the DVD Carriage Assy forward by turning its Worm clockwise, and remove the DVD Carriage Assy.
(3) Remove FPC Holder A and disconnect the PU flexible cable.

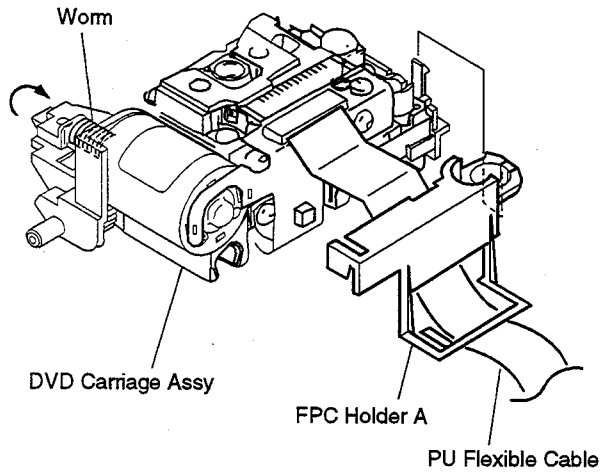


Fig. 1-13

- **Removal of the PU Holder Section**

(1) Place the two Carriage Assys in the PU Holder section.
(2) Disconnect the Flexible Cable from the TNMB Assy.
(3) Remove the four fixing screws ⑩ from the Turn Panel Assy.
(4) Remove the Cover S and disconnect the Flexible Cable from the Flexible Cable Cover.

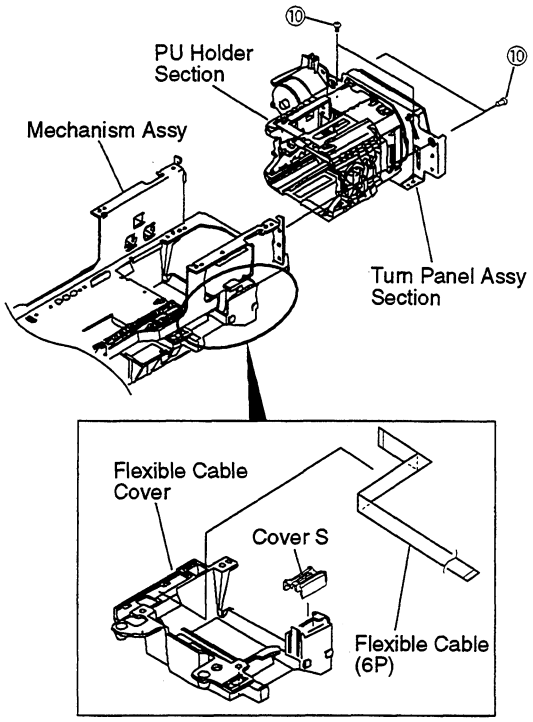
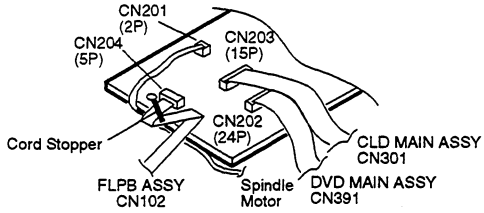
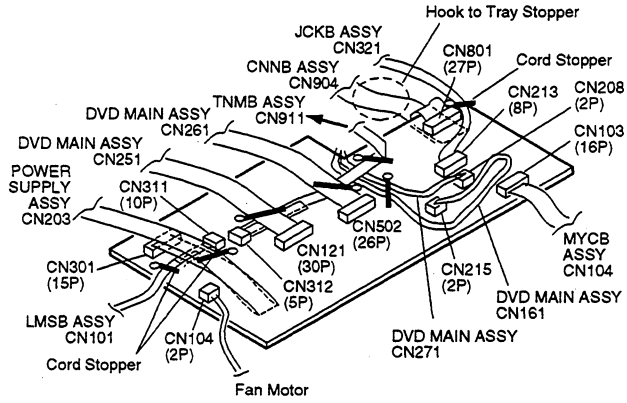


Fig. 1-14

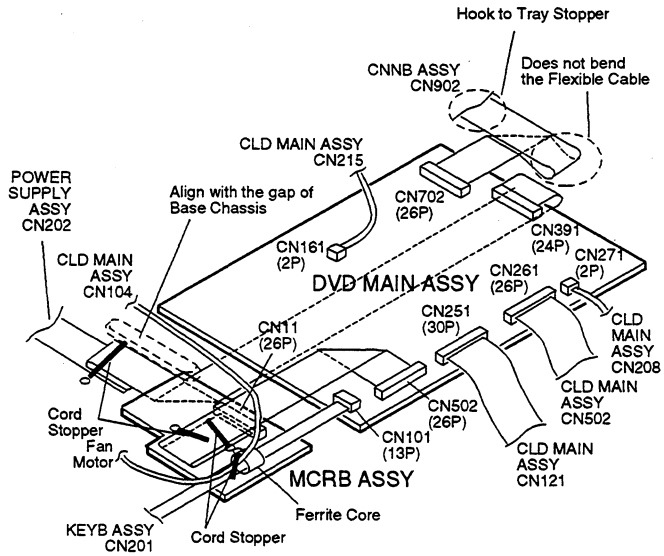
1.2.3 Style the Flexible Cable



• POWER SUPPLY ASSY



• CLD MAIN ASSY



• DVD MAIN ASSY, MCRB ASSY

Fig. 1-15

2. MECHANISM DESCRIPTION

2.1 NEW MECHANISM

(1) Skew Margin

The skew margin allowed for the DVD system is about half that allowed for the CD system, and the parallelism (between the optical pickup lens and the disc) required for the optical pickup drive is also critical. To secure the parallelism between the spindle motor fixing face and the guide bar fixing face for the optical pickup, 1.6-ton-rated sheet metal is used, achieving deviation in parallelism around half of that in the conventional CD specifications. In addition, use of sheet metal has enabled stable playback free of degradation caused by temperature changes, transportation and so on. However, this is not sufficient for the specifications required for the DVD system, so a newly developed tilting adjustment mechanism is also added. As for optical pickups for conventional CDs, titling adjustment against the drive is performed by the tilting adjustment mechanism of the actuator. For the optical pickup of the DVD system, a newly developed mechanism that adjusts the tilting of the entire optical pickup mechanism against the drive is used, which has resulted in a great improvement in parallelism and enable stable playback without a tilt servo mechanism. For the DVL-90 and DVL-700, a full use of the tilt servo mechanism, which is essential for playback of an LD, has yielded stable playback of DVDs.

(2) Disc Centering

Conventional CD players perform disc centering with a straight cylinder, detecting the inner periphery of a disc. Centering of a DVD must be done by the disc edge, because DVDs have a multilayered structure. For the DV-500, a mechanism that perpendicularly moves a cone-shaped centering hub and that has been used in conventional LD players is added for DVD centering. For the DVL-90 and DVL-700, this mechanism is already provided and can be also used for DVD centering.

(3) Spindle Motor

For DVD playback, a spindle motor for CD-ROMs and not for conventional CDs is required, because the rotation speed for a DVD is equivalent of four times that for CD-ROM. In addition, a brushless high-torque motor is used to secure full reliability as increases in axial looseness of the motor caused by a long use would induce inclination of the motor against the optical pickup, which would cause trouble in playback. For the DVL-90 and DVL-700, a spindle motor for conventional LDs is used.

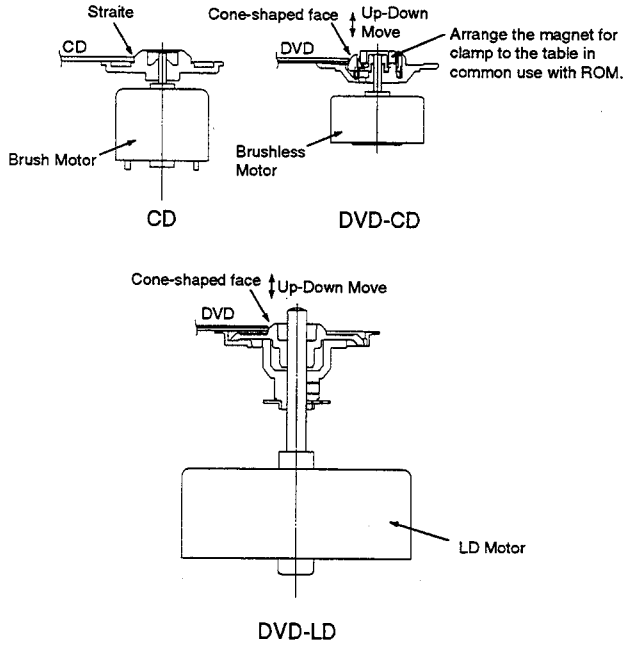


Fig. 2-1 Spindle Motor and Disc Centering

(4) Optical Pickup Positioning Mechanism

A high-speed search mechanism is essential for seamless playback such as multistory and multiangle playback. For the DV-500, a high-speed search mechanism used for CD-ROMs is used, with a backlashless high-speed gear mechanism used in quadruple-speed CD-ROMs, but with modifications for use with the DV-500 servo circuits.
Variable specifications required for DVD and CD-ROM (stable sequential playback for DVD and random-access response speed for CD-ROM) can be achieved only by changing the combination of gears in the same chassis, without changing the pitch between the motor and the guide shaft.
The optical pickup positioning mechanism for the DVL-90 and DVL-700 greatly differs from that for the DV-500.

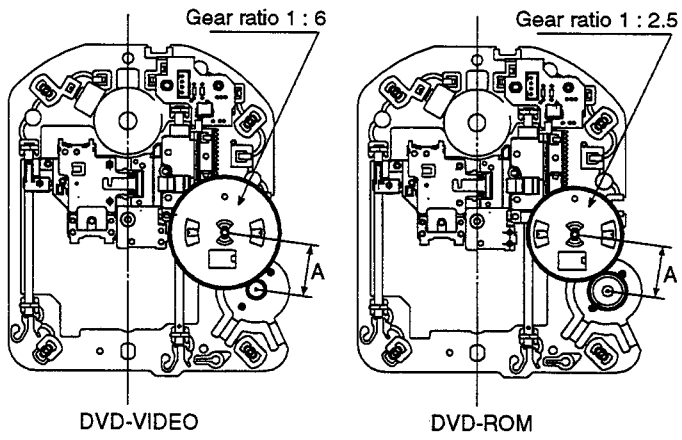


Fig. 2-2 Positioning Mechanism

2.2 MECHANISM OF DVL-90 AND DVL-700

(1) Optical Pickup Structure

One pickup for DVD playback and another pickup for playback of LDs and CDs are provided to perform one-side playback of DVDs, both-side playback of LDs, and playback of CDs.

The optical pickup used for LD playback is of proven quality. The optical pickup used for DVD playback is a dedicated one, which is equipped with an optical system required for DVD playback such as a high-NA-glass pressed lens and a short-wave length laser, as well as a motor mechanism for self-advancing, and a tilt sensor.

(2) Tray Unit Structure

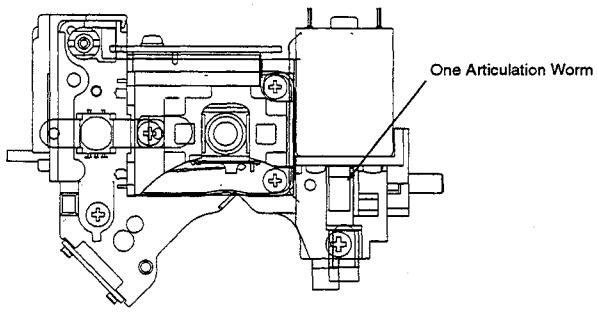
Two types of trays equipped with LD players as standard specification are provided: a tray for 12cm discs and a tray for 30cm discs.

A common carriage mechanism for LD player is shared between both trays.

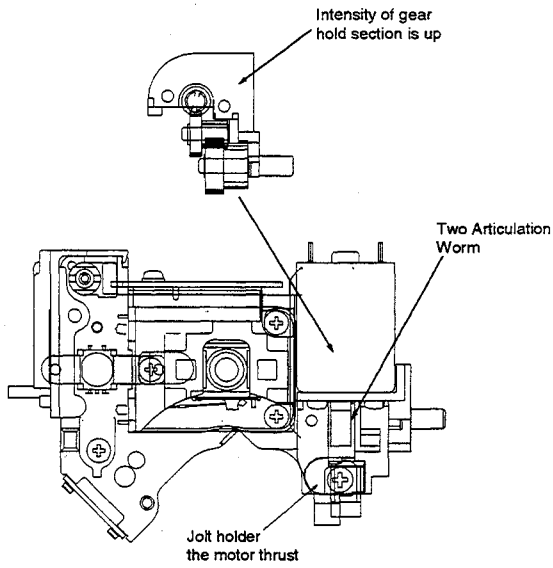
(3) Optical Pickup Changing Mechanism

One of the optical pickups is placed in the playback position according to the tray used, and another optical pickup is waiting at the rear of the Optical Pickup Positioning Mechanism. This waiting portion is a rolling mechanism that can house both optical pickups at the same time symmetrically at the upper and lower positions. When the optical pickup at the playback position is not the one for the type of disc to be played, this pickup is retracted to the Rolling Mechanism, and both optical pickups are rotated together by 180 degrees. Then, another optical pickup is moved to the playback position. For playback of side B of an LD, the optical pickup for LDs is rotated to side-B position, thus enabling seamless playback of both sides of an LD. Both optical pickups share the same guide bars, one provided for side A and the other for side B. For tracking of DVD playback, a one-beam tracking system is adopted. The Rolling Mechanism rotates with both pickups retracted. To reduce the rotation radius, a rotational fulcrum is separately provided, and the two pickups are together swung about 10 degrees and then rotated. For the Rolling Mechanism Drive, a dedicated motor is used for speedup of changing. At the same time, a motor drive that can function at twice the speed of conventional LD drives is provided for each pickup. In addition, a Tilt Servo Mechanism, which is essential for playback of LDs, is provided. This Tilt Servo Mechanism also enables stable playback of DVDs.

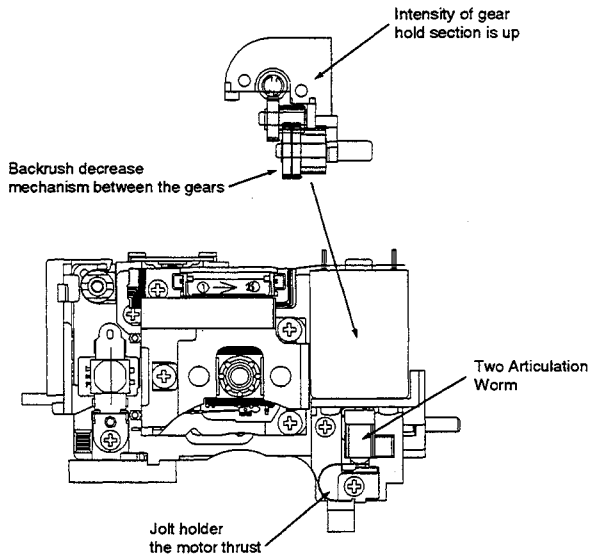
All these provisions for the Optical Pickup Positioning Mechanism add weight to the mechanism. Therefore, a Clamp Mechanism interlocked with the Tray Carriage Mechanism is newly employed for the protection of the Positioning Mechanism during disc removal and transportation.



Optical Pickup for Current LD



Optical Pickup for New LD



Optical Pickup for New DVD

Fig. 2-3 Optical Pickup Structures

(4) Optical Pickup-Positioning Mechanism

The feed rate of the self-advancing motor drives provided for the two optical pickups is twice that for conventional motor drives for LDs, because the feed rate for conventional motor drives for LDs is not sufficient for seamless playback. Associated with the speedup of the motor drive are an enhancement of the Gear Hold Section and a motor Thrust Adjuster. For the optical pickup for DVDs, a device to reduce backlash between gears is also provided.

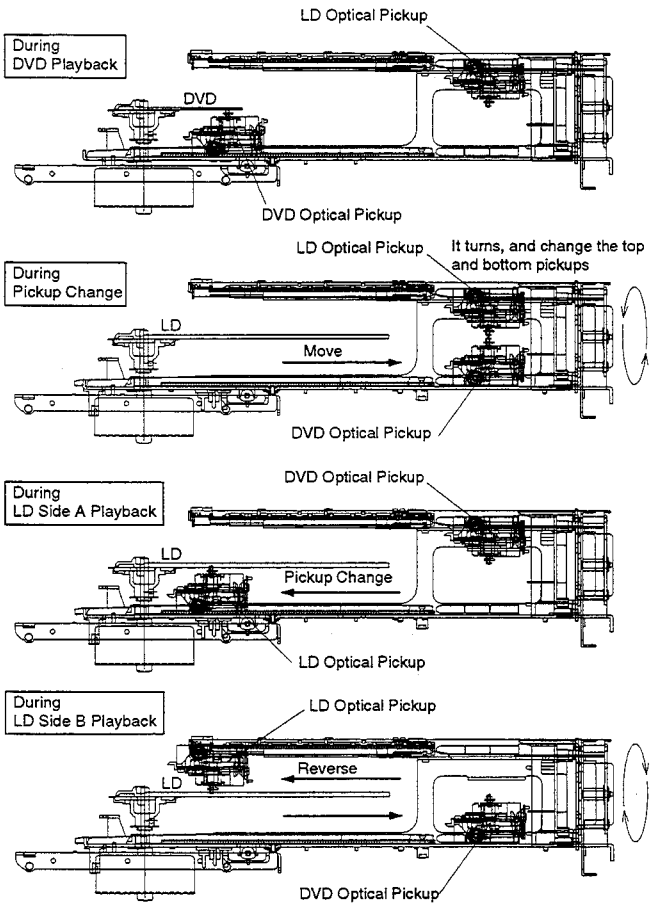


Fig. 2-4 Summary Diagram of Chang and Reverse the Pickup

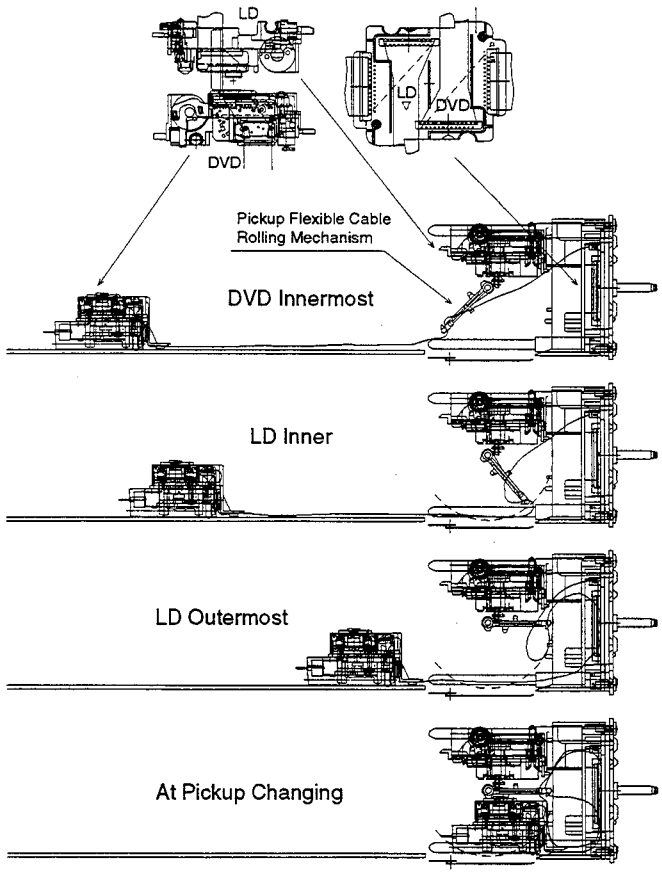


Fig. 2-5 Flexible Cable Store simulation during Pickup move

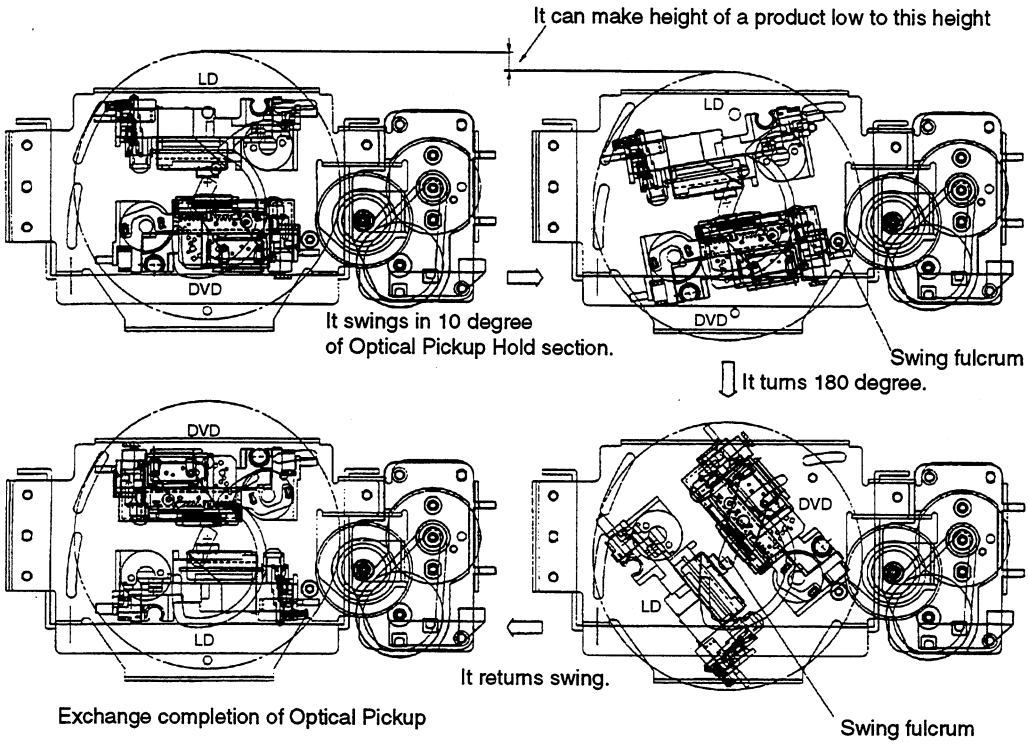
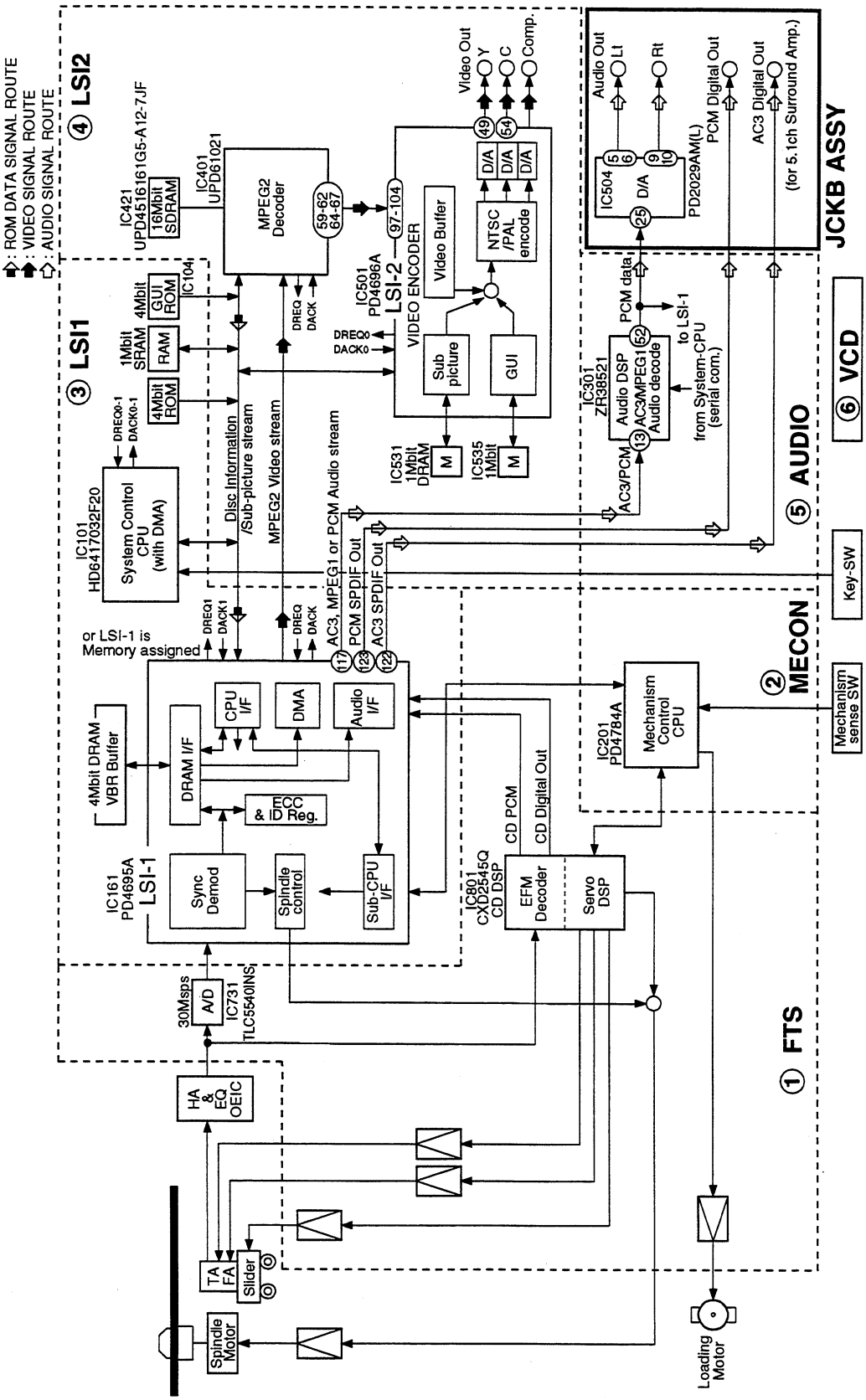


Fig. 2-6 Pickup Turning Mechanism Structure

3. ELECTRICAL DESCRIPTION

3.1 DV-500

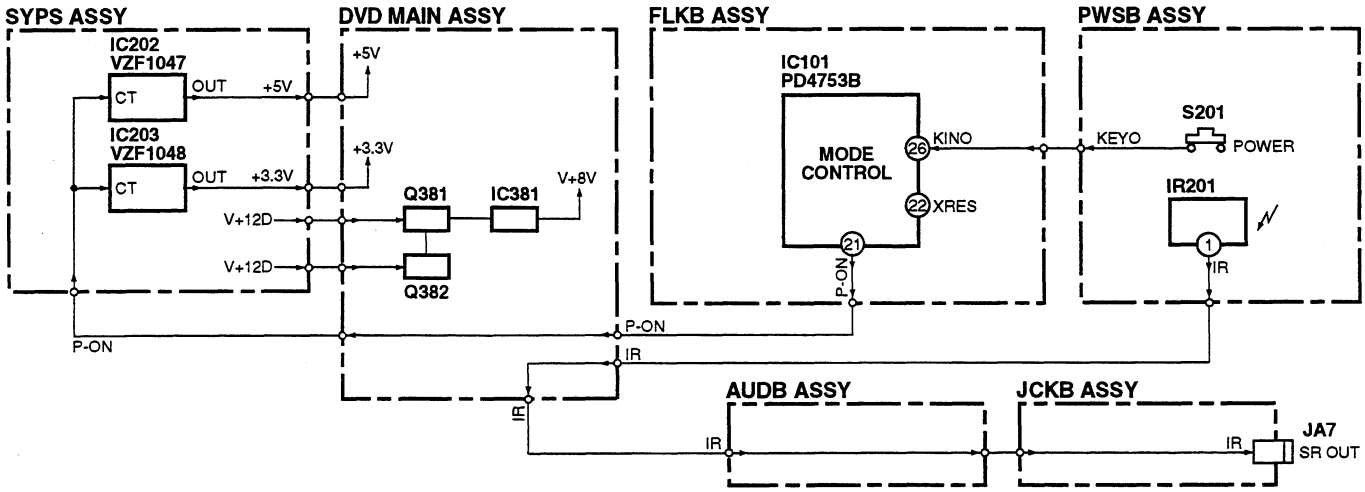
3.1.1 OVERALL BLOCK DIAGRAM



3.1.2 OPERATIONS

(1) P-ON

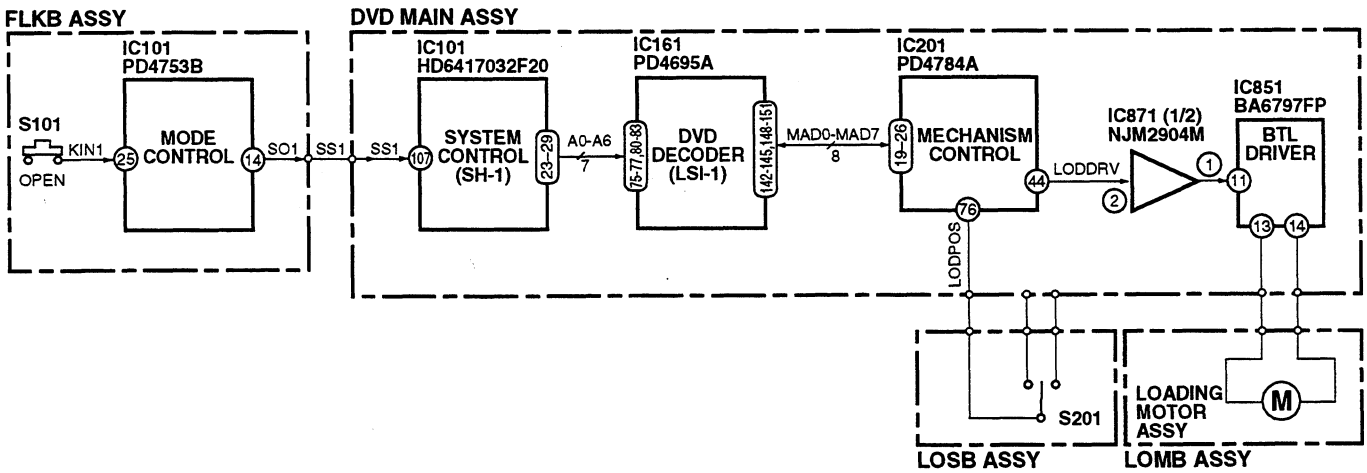
When the P-ON command is sent from a button on the remote control unit or on the main unit, the FL control computer (PD4753B) responds to the command. First, pin 21 (POWER ON) is set to H so that 5 V and 3.3 V of the SYPS Assy and 8 V of the DVD MAIN Assy are on. Then, pin 22 (XRES) is set to H so that each IC is released from reset status and initialized.



(2) Loading

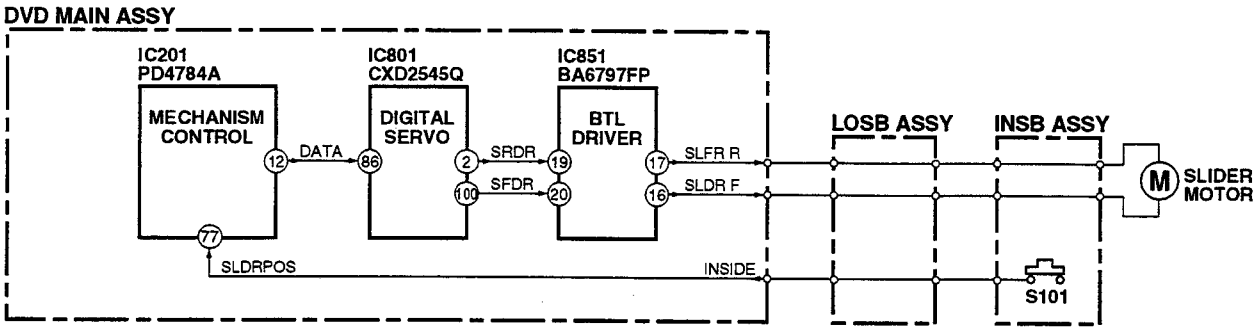
When the FL control computer (PD4753B) recognizes the OPEN command, it transfers the corresponding data serially to the system control computer (SH-1.) When receiving the data, SH-1 translates the mode and writes the corresponding operation command to the data memory of LSI-1 through an address bus. This operation command is transferred to the mechanism control computer (PD4784A) through an address data bus. (Other operation commands such as PLAY and SEARCH are also transferred from SH-1 to the mechanism control computer through LSI-1 in the same way.)

Once receiving the command, the mechanism control computer controls the loading motor via pin 44 (LOAD DRV) while monitoring pin 76 (LOAD POS) in the following manner: the PWM output from pin 44 goes through the OPAMP (IC871) and controls the motor with the Motor Driver BA6797FP (IC851.) Thus, the disc is set into the main unit.



(3) Slider Movement into the Minimum Internal Circumference

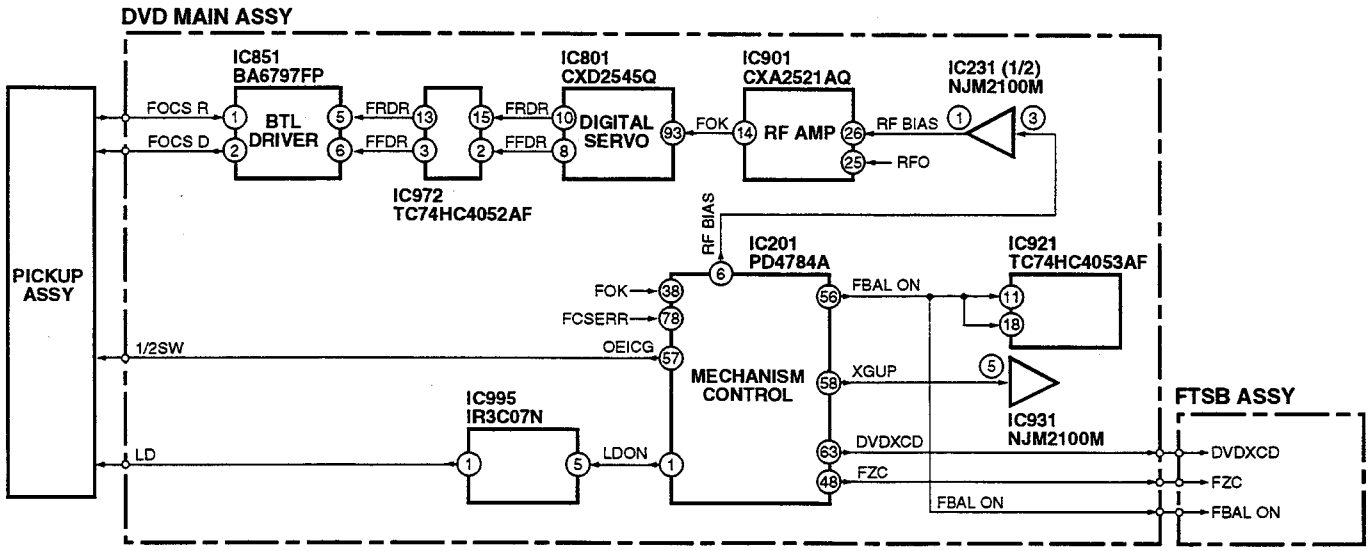
When a disc is loaded, the mechanism control computer orders the pickup to move to the minimum internal circumference, which is the disc-sensing position, while monitoring pin 77 (SLDR POS.) This movement to the minimum internal circumference is performed by the mechanism control computer, which sends serial data to Digital Servo IC CXD2545Q (IC801). CXD2545Q, corresponding to the Slider Drive command, outputs the PWM signal from pin 2 and pin 100 (SLDR DRV), and through the Motor Driver, causes the Slider Motor to move.



(4) Disc Sensing

At the next step, disc sensing is performed by the mechanism control computer. As the initial setting, the following settings are made: Pin 57 (OEIC GAIN) = L; pin 58 (XGAIN UP) = H; pin 56 (FBAL ON) = L; pin 48 (DVD/XCD) = H. Then pin 1 (LD ON) is set to H so that the LD Driver IR3C07 (IC995) is activated to light LD ON. Then the lens is moved to its highest position in response to the FCS DRV signal from pins 8 and 10 of CXD2545Q. The above actions are all ordered by the mechanism control computer. At this stage, pin 6 (RF BLAS) of the mechanism computer outputs the offset correction to cancel offset of RFO (IC901 pin 25.).

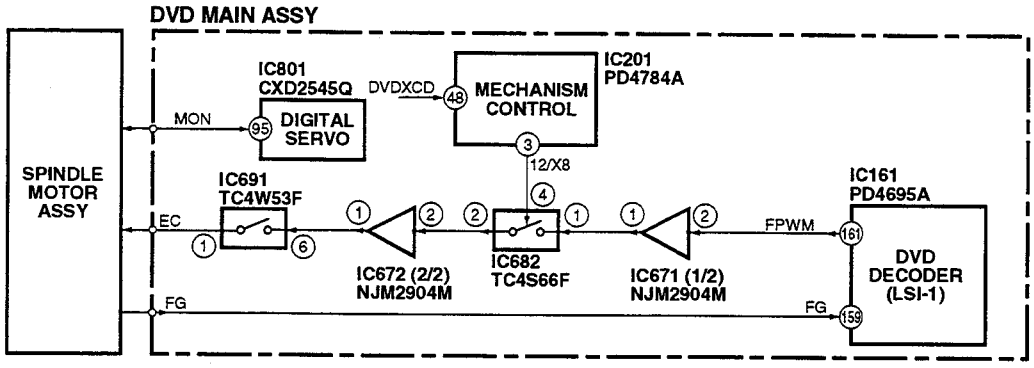
The lens then moves down at a constant speed, and the disc sensing starts when the following conditions are satisfied: Pin 63 (FZC) of the mechanism control computer = L and pin 38 (FOK) = H. Disc sensing is conducted using the sinewave signal from pin 78 (FCS ERR) of the mechanism control computer. As the level of the reflected light differs depending on the disc to be played back, to obtain the optimum level, after the first sweep, OEIC GAIN is set to H and after the second sweep, XGAIN UP is set to L. Sweep is conducted a maximum of three times. If the conditions FZC = L and FOK = H are not satisfied after the third sweep, the status is judged as NO DISC.



(5) Disc-Size Sensing (8 cm/12 cm)

After disc sensing, disc-size sensing is performed. The disc size is sensed by rotating and accelerating the spindle motor and by calculating its rotation speed and time as follows: First, the Motor-On command is transmitted to CXD2545Q, which sets pin 95 (MON) to H and activates the drive circuit of the spindle motor; At the same time, the Acceleration command is transmitted to LSI-1, and the PWM signal for the FG servo for maximum acceleration is output from pin 161 (FPWM); The FPWM signal, passing via IC671 and IC672, orders acceleration at the motor; To obtain data on the motor's rotation speed, the mechanism control computer reads the FG pulse, which is output from the motor and input to pin 159 (FG) of LSI-1.

Thus, disc-size sensing is completed, and the setting of pin 3 (8/X12) and pin 48 (DVD/XCD) of the mechanism control computer are completed



(6) CD Focus-In

First, the spindle motor is rotated, and the disc is turned. To do this, unlike the case of disc sensing, CXD2545Q is used, because the analog switch of IC691 has been set to the side of pin 7 in response to the DVD/XCD signal. Pin 95 (MON) of CXD2545Q is set to H to activate the motor, and the SPDL ERR signal is output from pin 96 (MDP.) The MDP is at first accelerated in Kick mode up to 600 rpm. If the rotation speed exceeds 600 rpm, the mechanism control computer sets the unit to STOP mode and switches the MDP to HI-ZI, which puts the motor in Free-Run mode. The lens moves to the lowest position after LD ON because the drive direction of the FCS is reversed by IC972. Then, the mechanism control computer sets pin 55 (F SHUNT) to H and shunts the FCS ERR signal on the way to CXD2545Q by Q946. This is to prevent focusing in with noise before a real sinewave signal or pseudo-sinewave signal. Then the mechanism control computer sends the Auto-Focus command to CXD2545Q. The lens moves up at constant speed. The mechanism control computer, which monitors pin 78 (FCS ERR) at the same time, sets pin 55 (F SHUNT) to L when the peak of a sinewave signal exceeds the threshold value that was set upon disc sensing. FCS LOOP is set to ON if the following two conditions are met: the FE of the trailing edge of the sinewave signal crosses the zero point, and pin 93 (F OK) of CXD2545Q is set to H.

(7) CD Startup

The mechanism control computer recognizes FCS ON by monitoring pin 80 (SENS) of CXD2545Q and orders the pickup to move to the outer periphery by a certain distance. Then, it starts Auto Tracking Balance (ATB). In performing ATB, pin 42 (ATB ON) is set to H, and the LPF SW (Q811) of the TE is set to ON, which sets the DC offset value of the TE written as a register value inside CXD2545Q and corrects the offset value to become 0 with pin 5 (ATB DRV). Then AGC is performed. FCS and TRKG are conducted by CXD2545Q. The RF level is controlled so that the level of the RF signal, which is converted from analog to digital at IC 731 and then input via pins 200-207 of LSI-1, is kept constant by controlling the RF amplifier gain of Q714 variably with OUT 0-OUT 3. Then TOC Read and PLAY are performed.

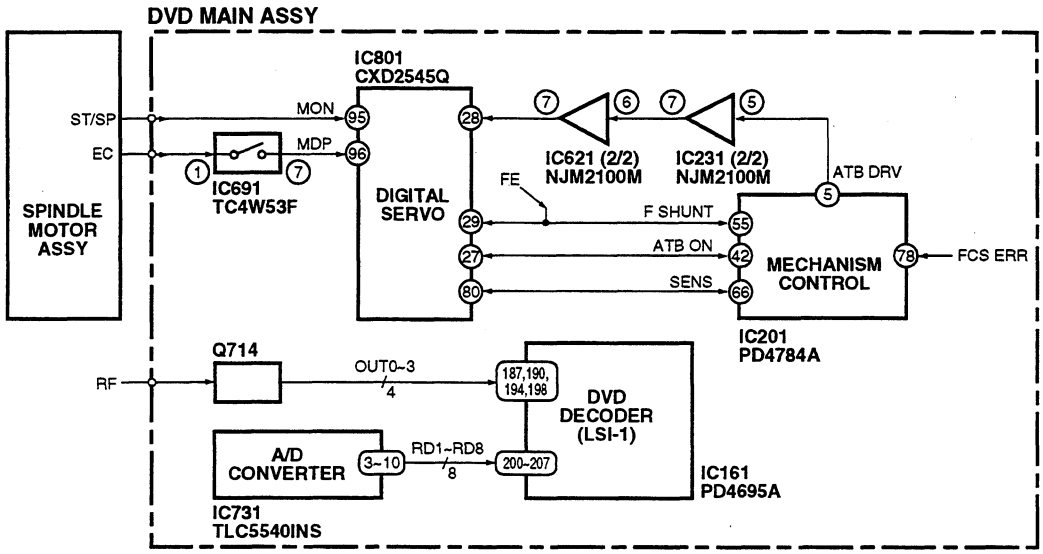
(8) DVD Focus-In

Most of the DVD Focus-In operations are the same as those for a CD, except for following two points:

(1) The sweep direction for focusing is reversed; i.e. the sweep direction is the same as that for disc sensing.
(2) the spindle motor is not rotated for focusing.

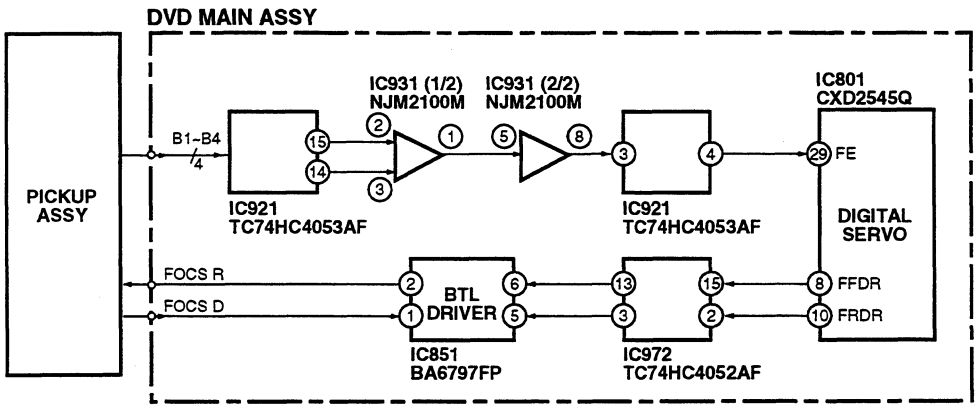
(9) DVD Startup

DVD startup operations are mostly the same as those for a CD, except the following: The rotation of the spindle motor is performed after FCS ON, ATB and AGC are conducted without moving the pickup, and NAVI Information Reading and PLAY are then performed.



(10) Focus Loop

The photodetector signal is divided into signals B1, B2, B3, B4, which are output by the OEIC of the pickup and sent through the Focus Balance switch of IC921 and converted into the FCS ERR signal at the FE AMP of IC931. This FCS ERR signal is then input via pin 29 of the Digital Servo IC (CXD2545Q), where the signal is internally processed, and the FCS DRV signal is output from Pins 8 and 10, and the Focus Servo is driven by the Driver Amplifier of IC851.

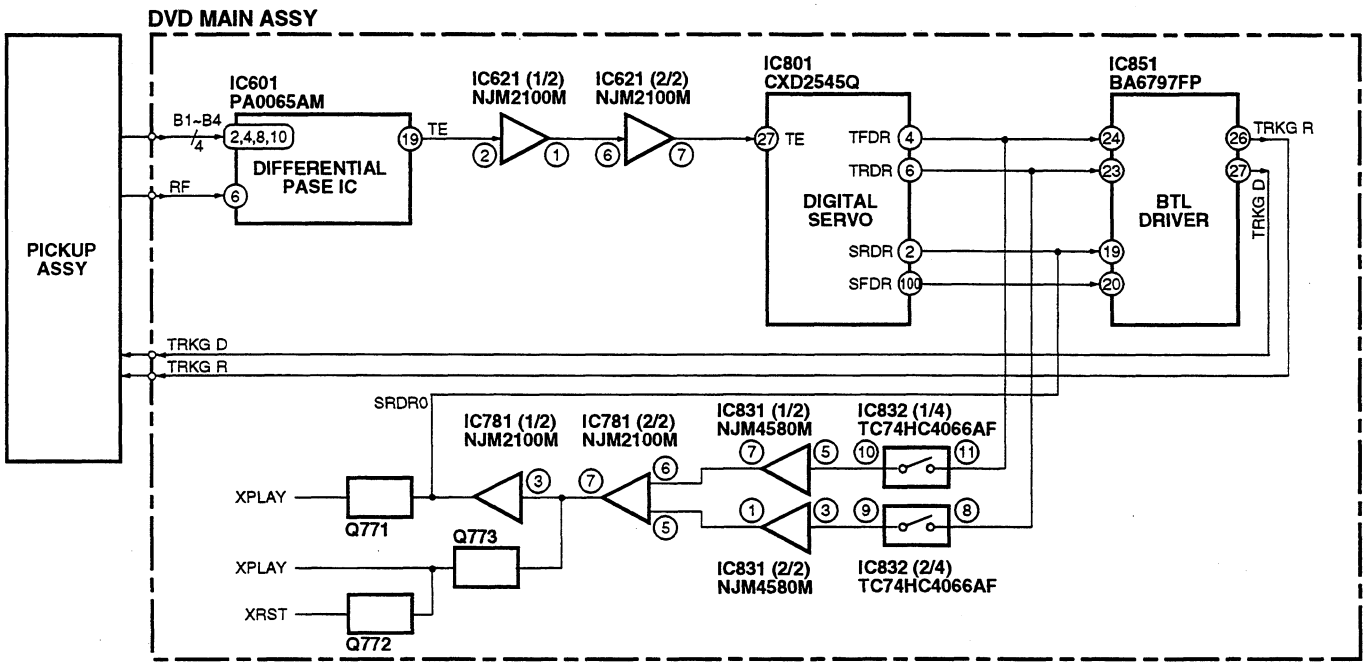


(11) Slider Loop

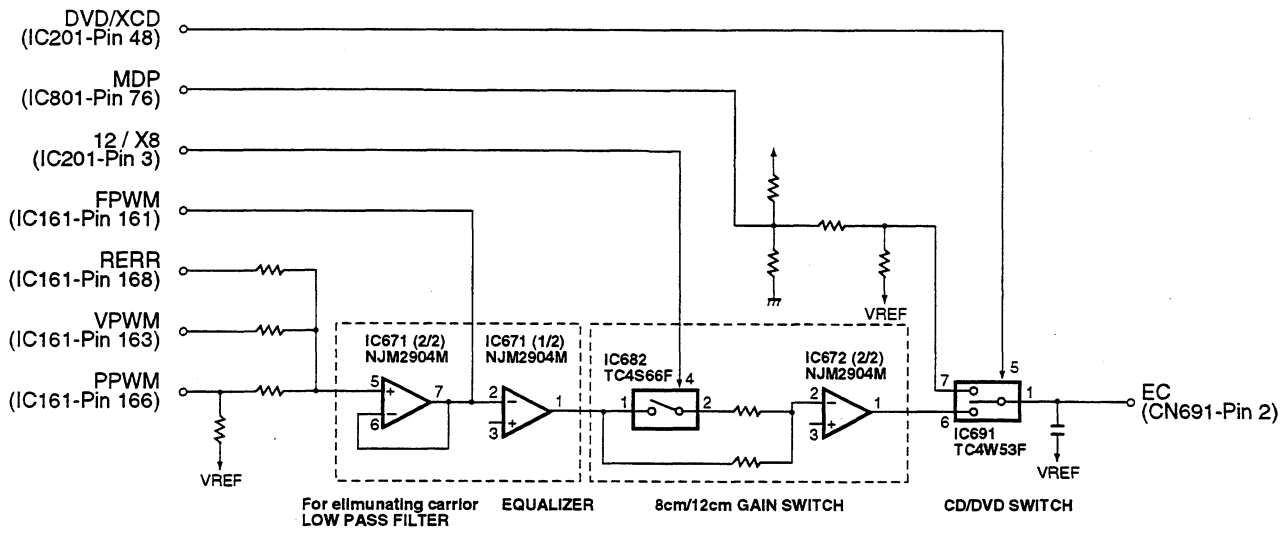
The Slider Error signal is output from pins 4 and 6 (TRK DRV output) of Digital Servo IC. The Slider Error signal, which goes through the Slider Error Amplifier (IC781) is mixed with the signal from pins 2 and 100 (slider control output) of the Digital Servo IC at the Driver Amplifier (IC851) and drives the slider. Q771 and Q773 are loop switches.

(12) Tracking Loop

The TE signal is formed when the B1, B2, B3, B4 signals output from OEIC of the pickup and the RF signal are input to the Time-Difference-TE-Forming IC (IC601.) The TE signal, output from pin 19, to which the offset signal is added in IC231, is then input via pin 27 of Digital Servo IC (CXD2545Q). The signal is then digitally processed, and the Kick Brake Pulse is switched, and the TRKG DRV signal is output from pins 4 and 6. The Tracking Servo is then driven by the Driver Amplifier (IC851.)



(13) Spindle Servo Block



IC161	FPWM (Pin 161)	RERR (Pin 168)	VPWM (Pin 163)	PPWM (Pin 166)
at Stop	duty 50%	Z	Z	Z
at Acceleration	duty 99%	Z	Z	Z
at Lock	Z	Z	about 50%	about 38%
at Deceleation	duty 0%	Z	Z	Z
Carrier Frequency	55kHz	—	104kHz	167kHz

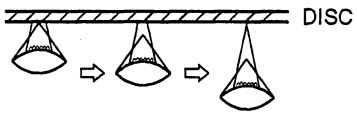
"Z" : High Impedance

In actual usage, rough servo status caused by the RERR signal is very short, and few cases can be identified clearly.
For a setting sake, rough servo is a transitional status from the FG servo to the Speed/Phase servo. As for gain switching for 8 cm/12 cm, the gain is decreased for an 8-cm disc by increasing the input resistance of the IC672 Operation Amplifier. Conversely, the gain is increased for a 12-cm disc by parallel connection of the input resistance.
Switching between a CD and DVD is done by IC691 with the MDP output and the DVD/XCD output for CDs from CXD2545Q.
The FG pulse is output from the open collector of the motor only if pin 95 (MON) of IC801 (CXD2545Q) is set to "H." The FG pulse pulled up with R699 4.7 kΩ is input to pin 159 of IC161(LSI-1.)
The number of FG pulsed is 6 per rotation.

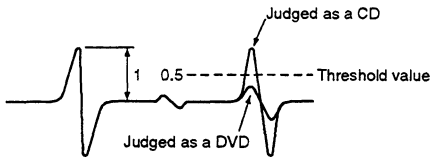
(14) Basic Method for Disc Sensing

• Disc sensing

① Lens sweep
Up → Down



② FOCS sinewave output signal
Judged by the ratio of first-order sinewave to 0-order sinewave



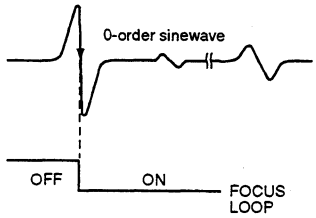
<0.5 : Judged as a DVD
≥0.5 : Judged as a CD

Note : The pseudo-sinewave signal is not blinded.

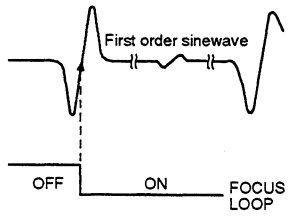
• Focus-in

FZC : Looped in with the first sinewave signal

① DVD disc Lens sweep Up → Down



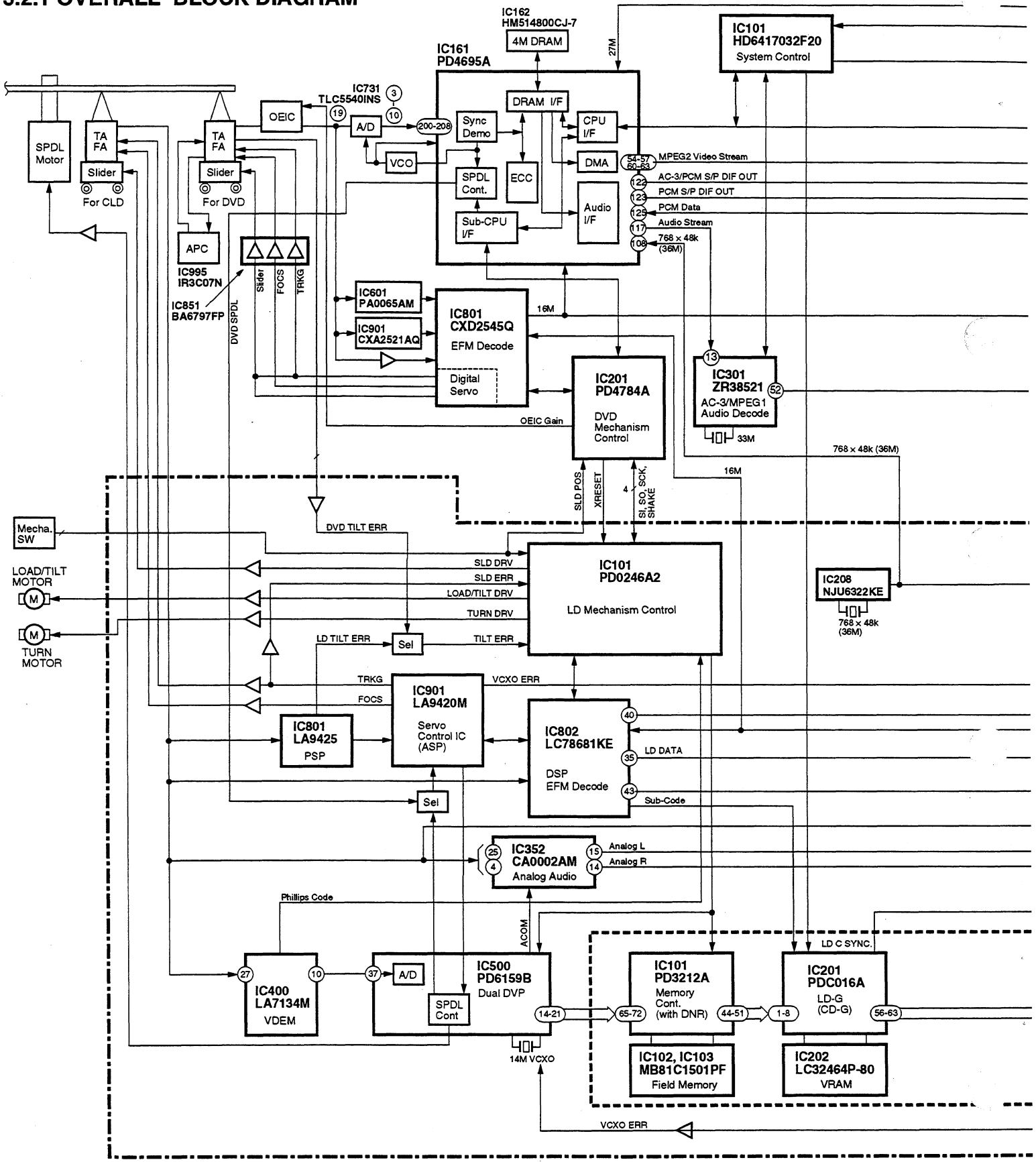
② CD disc Lens sweep Down → Up

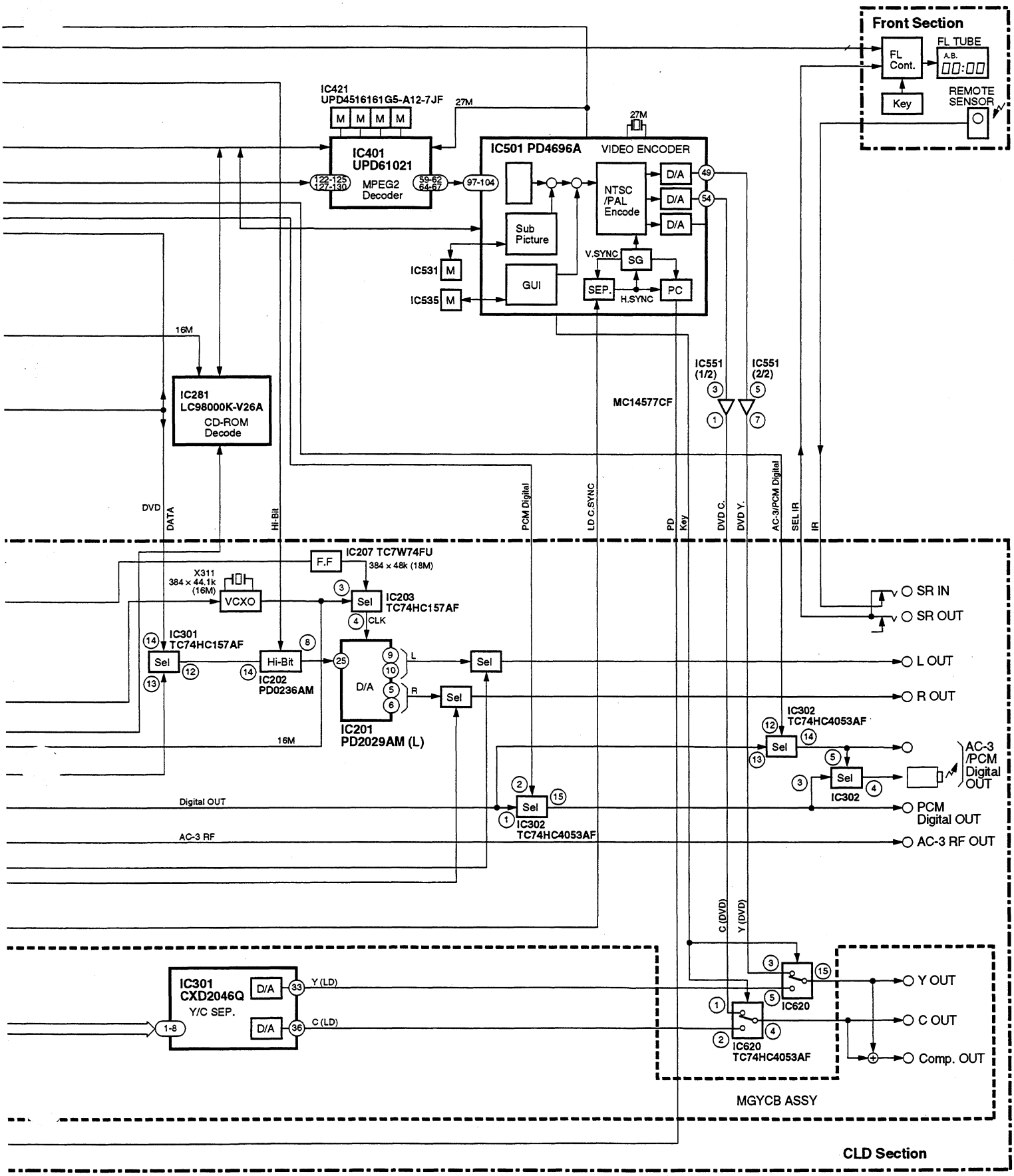


Note : Change the detecting edge direction

3.2 DVL-90 AND DVL-700

3.2.1 OVERALL BLOCK DIAGRAM




Front Section
FL TUBE
FL Cont.
A.B.
Key
REMOTE SENSOR
IC421
UPD4516161G5-A12-7JF
27M
IC401
UPD61021
MPEG2 Decoder
122-125
127-130
59-62
64-67
97-104
IC501 PD4696A
VIDEO ENCODER
NTSC /PAL Encode
D/A
49
54
Sub Picture
GUI
V.SYNC
SG
SEP.
H.SYNC
PC
IC531
IC535
16M
IC281
LC98000K-V26A
CD-ROM Decode
IC551 (1/2)
IC551 (2/2)
MC14577CF
DVD
DATA
Hi-Bit
PCM Digital
LD C.SYNC
PD
Key
DVD C.
DVD Y.
AC-3/PCM Digital
SEL IR
IR
F.F
IC207 TC7W74FU
384 x 48k (18M)
X311
384 x 44.1k
(16M)
VCXO
Sel
IC203
TC74HC157AF
CLK
IC301
TC74HC157AF
Hi-Bit
IC202
PD0236AM
D/A
L
R
IC201
PD2029AM (L)
SR IN
SR OUT
L OUT
R OUT
IC302
TC74HC4053AF
AC-3 /PCM Digital OUT
PCM Digital OUT
AC-3 RF OUT
Digital OUT
AC-3 RF
C (DVD)
Y (DVD)
IC301
CXD2046Q
Y/C SEP.
Y (LD)
C (LD)
IC620
IC620
TC74HC4053AF
Y OUT
C OUT
Comp. OUT
MGYCB ASSY
CLD Section

3.2.2 OPERATIONS

(1) Loading

In Compatible-Model mode, a command is serially transmitted from the DVD mechanism control computer to the CLD mechanism control computer. The CLD mechanism control computer controls the Loading Motor [Motor Driver IC803 (2/2)] with the PWM output from pin 24 (TILT OUT) while monitoring pins 33-35 (SW1, SW2, SW3).

(2) Slider Movement Toward the Inner Periphery

Once a disc is loaded, the DVD mechanism control computer orders the pickup to move to the disc-sensing position while monitoring pin 77 (SLDR POS). (The location of the disc-sensing position is decided by moving the pickup from the outer periphery to the inner periphery and again to the outer periphery to avoid sensing the turntable. In this case, the setting of the INSIDE SW is ignored.)
The subsequent operations are the same as those of the DV-500.

(3) Disc Sensing

Disc sensing is performed with the two pickups of the DVL-90 and DVL-700.

• CLD Pickup Side

A disc that is focused in at the LD sensing position is recognized as an LD.
When a disc is focused in at the CD sensing position, whether the disc is a DVD or CD is judged according to the TZC as follows:
After Focus-In, the disc is rotated, and its disc type is judged by the number of the TZC within a rotation at a specific rotation speed. The TZC is a signal in which a TE signal, via the LPF, comparator IC907 (1/2) and the switch (IC761), is input to pin 22 of the CLD mechanism control computer. If TZC $\geqq$ 5, the disc is judged to be a CD, and if TZC<5, the disc is judged to be a DVD.
If focusing is not successful at the CD sensing position, the mechanism control computer, through pin 53, monitors pin 16 of the PSP (IC801) and judges whether a disc is loaded or not.
If the DEFO is kept at L for more than 2 ms during sweeping, it is judged that a disc is loaded, and the DVD pickup will be used. If the DEFO remains at H, it is judged that no disc is loaded.
(Failure to focus in with a disc loaded is often caused by a dual-layered disc.)

• DVD Pickup Side

The DVL-90 and DVL-700 performs disc in/out sensing with the Tilt Sensor output and disc-type sensing by using the FE and sinewave signals. Sensing with the Tilt Sensor is required in addition to the DV-500 procedures to avoid judging as NO DISC when a sinewave signal is not detected with a CD-R disc. The method for judging DVD/CD is the same as with the DV-500, except for the following point: During the third sweep, in a case where the DV-500 would make a judgment of NO DISC, the DVL-90 and DVL-700 monitors pin 53 (Disc In/Out port) of the CLD mechanism control computer. If the port indicates that a disc is loaded, the DVL-90 and DVL-700 judges the disc as a CD-R and changes pickups.

(4) Disc-Size Sensing (8 cm/12 cm)

This procedure is not performed, because the DVD mechanism does not switch the spindle gain for 8 cm/12 cm.

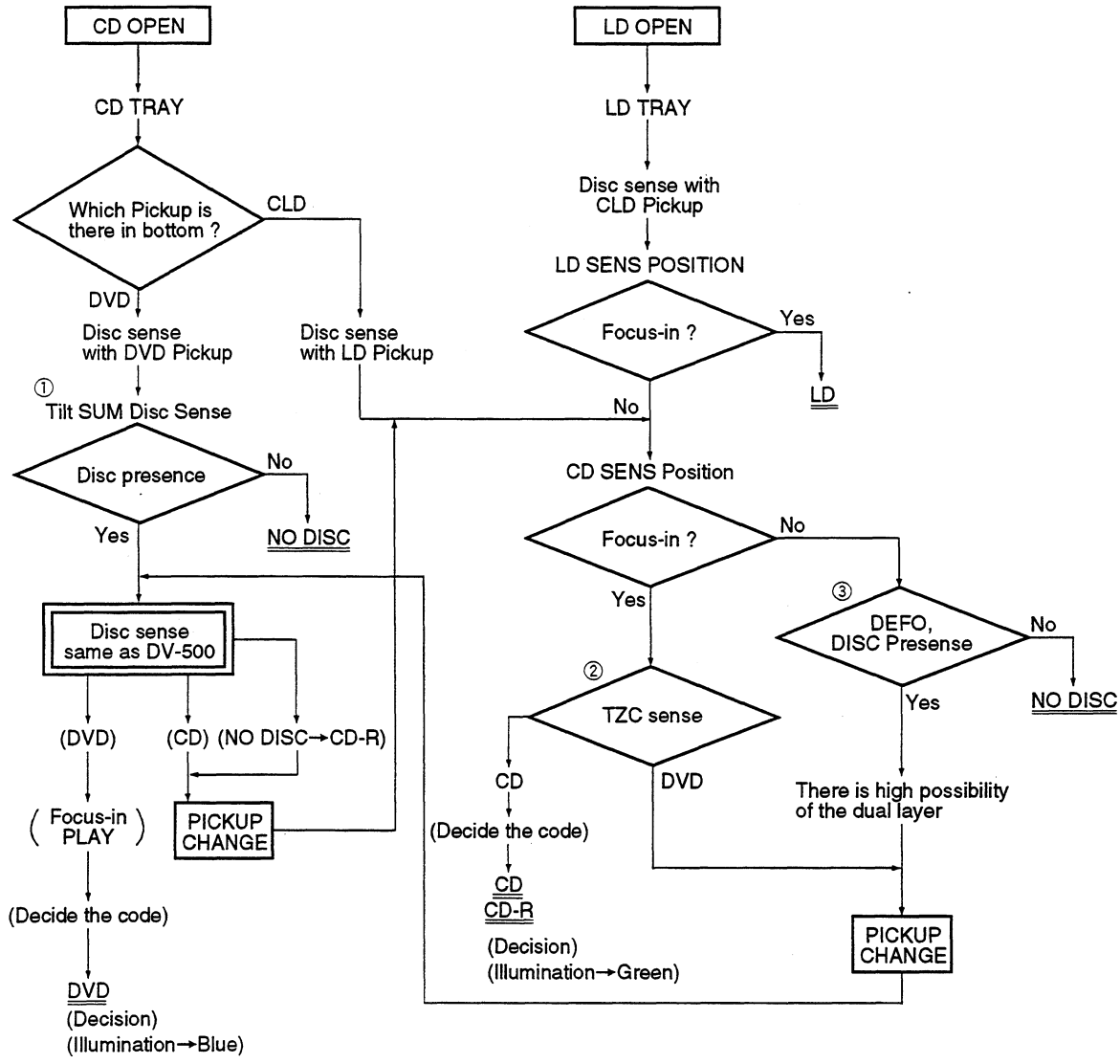
(5) Differences from the DV-500

The following operations are added to correspond to CD-R discs and because the CLD pickup is added:

① Judgment of DISC IN/OUT with the DVD pickup tilt sum (because sinewave signal output is not reliable with CD-R discs)

② Judgment of DVD/CD according to the TZC signal during the CLD pickup operation

③ Judgment of DISC IN/OUT with the DEFO during the CLD pickup operation



4. TEST MODE

4.1 HOW TO ENTER/EXIT FROM TEST MODE

How to enter : To enter SD Test mode, press the ESC key then the TEST key on the remote control unit. In SD Test mode, corresponding information will be displayed on the blue back screen.

How to exit : Press the ESC key while in SD Test mode.

4.2 TEST MODE OPERATIONS

Command	Condition	Key (Remote Control Unit)	Mode of the Remote Control Unit
Open	STOP	REPEAT A	A8-48
Close	OPEN	REPEAT A	A8-48
Stop	PLAY	REPEAT B	A8-44
Play (startup the spindle)	STOP	TV/LDP	A8-0F
Pause (still picture)	PLAY	CX	A8-0E
Search address input (0– 9)		0~9	A8-00– 09
Search address input (A– F)	While entering an address	PGM+1 – 6	
①Search address crear ②Exit from Search input mode	While entering an address Address = 0	CLEAR	A8-45
①To enter Search address input mode ②Change of address input methods (Absolute address→Addition→Subtraction)		+10	A8-1F
Search excution		CHAP/TIME	A8-13
Tracking open	PLAY	STEP FWD	A8-54
Tracking close	PLAY	STEP REV	A8-50
Slider in	TR : Off	SCAN REV Shuttle REV	A8-11 A8-2C– 2F
Low speed scan REV	TR : On	SCAN REV	A8-11
Scan REV (x4, x8, x16, x32)	TR : On	Shuttlr REV	A8-2C– 2F
Slider out	TR : Off	SCAN FWD Shuttle FWD	A8-10 A8-28– 2B
Low speed scan FWD	TR : On	SCAN FWD	A8-10
Scan FWD (x4, x8, x16, x32)	TR : On	Shuttle FWD	A8-28– 2B
Loading in	STOP	SKIP REV	A8-53
Loading out	STOP	SKIP FWD	A8-52
Tilt neutral		SPEED DOWN	A8-46
Tilt servo on		SPEED UP	A8-47
Tilt servo off	Tilt : On/N	SKIP REV SKIP FWD	A8-53 A8-52
Tilt up	PLAY	SKIP FWD	A8-52
Tilt down	PLAY	SKIP REV	A8-53
LD on		TEST + 1	A8-5E + A8-01
Focus on		TEST + 2	A8-5E + A8-02
Focus sweep		TEST + 3	A8-5E + A8-03
Focus jump +		MULTI FWD	A8-58
Focus jump –		MULTI REV	A8-55
Turn B	CLOSE	SIDE-B	A8-4E
Turn A	CLOSE	SIDE-A	A8-4D
Spindle auto servo		TEST + 4	A8-5E + A8-04
Spindle FG on		TEST + 5	A8-5E + A8-05
Spindle PLL on		TEST + 6	A8-5E + A8-06
AGC on	AGC : Off	TEST + 7	A8-5E + A8-07
AGC off	AGC : On	TEST + 7	A8-5E + A8-07
ATB on	ATB : Off	TEST + 8	A8-5E + A8-08
ATB off	ATB : On	TEST + 8	A8-5E + A8-08
Indication of the coefficient of CXD2545Q		TEST + 9	A8-5E + A8-09
CD error rate indication	CD PLAY	TEST + 0	A8-5E + A8-00
Screen display on (Switching of Ver. and Rev. indications)	OSD : Off/On	DISPLAY	A8-43
Screen display off	OSD : On	AUDIO	A8-1E
Screen display on/off		PROGRAM	A8-4C
Switching of ID display methodes (decimal/hexadecimal)		DIG/ANA	A8-0C
Disc type designation • Forced designation to DVD • Forced designation to CD • Request for Disc sensing	STOP	HILITE/INTRO + 1 + 3 + 0	A8-5A + A8-01 + A8-03 + A8-00
Tray close of disc sense inhibition	Checker mode	REPEAT A	A8-48

4.3 NOTES

(1) For measuring the DVD error rate, simultaneously press the ESC and PLAY keys while in the normal status. The DVD error signal is then serially output from LSI-1 in sequence during playback.

(2) Indications for the spindle status are as follows:
A/B : Spindle accelerator and brake
FG : FG servo
SRV : Rough, velocity/phase servo
O_S : Offset addition, rough, velocity/phase servo

(3) There are three methods for entering a search address:
① Absolute address designation
→Searching for the address entered
(indication for the most significant digit : >)
② Additional input
→Searching for the address with the current ID number plus an entered number
(indication for the most significant digit : +)
③ Subtractive input
→Searching for the address with the current ID number minus an entered number
(indication for the most significant digit : -)
The above modes can be changed by pressing the +10 key.

Note : A number for addition or subtraction must be entered in hexadecimal.

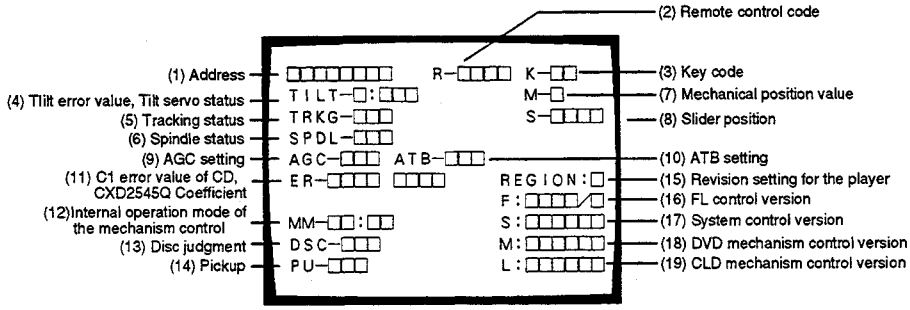
(4) If you turn the power on while short-circuiting the short-circuit terminal at the side of the system control computer, the unit will forcibly enter Test mode. If the FL control computer is set to Checker mode, disc sensing will not be started, even if a disc is loaded. Disc sensing will also not be performed if the tray is opened/closed by your pressing REPEAT A key while in Checker mode. However, disc sensing will be started if the OPEN/CLOSE key on the main unit or on the remote control unit is pressed.

(5) If disc-type designation is forcibly executed during a mode other than Checker mode, the system control computer will abandon disc-type designation after setting the mechanism control computer. Therefore, after startup of the unit, disc sensing will be performed again for safety. If disc-type designation is forcibly executed during Checker mode, as disc-type designation is not abandoned, playback will be immediately started.

4.4 TEST MODE DISPLAY SPECIFICATIONS

Consecutive single-OSD display is supported during Test mode. The screen is composed 10 lines with a maximum of 24 characters per line. Simultaneous use of RAM Display mode or Debug Display mode cannot be performed.

4.4.1 Screen Composition



4.4.2 Description of Each Item on the Display

(1) Address indication
The address being traced is displayed in number:
DVD : ID indication [********]
(hexadecimal number, 8 digits)
CD/LD (CLV) : A-TIME (min. sec.) [○○○○ ****]
LD (CAV) : FRAME [○○○ *****]
(Note : For DVDs, decimal-number indication is possible.)

(2) Key code indication for the remote control unit [R–****]
The code for the key pressed on the remote control unit, which is received by the FL control computer, is displayed while the key is pressed. In the case of the double code, the second code will be displayed.

(3) Key code indication for the main unit [K–**]
The code for the key pressed on the main unit, which is received by the system control computer, is displayed while the key is pressed.

(4) Tilt error value, Tilt servo status [TILT–*:***]
Tilt error value : [0]–[F]
Tilt servo status : Tilt neutral [N]
Tilt servo on [ON]
Tilt servo off [OFF]

(5) Tracking status [TRKG–***]
Tracking on : [ON]
Tracking off : [OFF]

(6) Spindle status [SPDL–***]
Spindle accelerator and brake : [A/B]
FG servo : [FG]
Rough, velocity/phase servo : [SRV]
Offset addition, rough, velocity/phase servo : [O_S]

(7) Mechanism position value [M–*]
Position code : [0]–[8]

(8) Slider Position [S–****]
CD TOC area : [IN]
CD active area : [CD]
CDV video area : [CDV]
LD active area : [LD]
Side B inside : [B IN]

(9) AGC setting [AGC–**]
AGC on : [ON]
AGC off : [OFF]

(10) ATB setting [ATB–**]
ATB on : [ON]
ATB off : [OFF]

(11) Indications for the following two types of information can be switched:
① C1 error value of CDs [ER–C1****]
C1 error value of CDs (up to four digits)
(Note: Error value indication for DVDs cannot be used.)
② Q coefficient for CXD2545Q [KS–[**]****]
The address for the designated coefficient (2 digits) and its setting number (4 digits) are displayed.

(12) Internal operation mode for the mechanism control computer [MM–** : **]
Internal mechanism mode (2 digits) and internal mechanical step (2 digits) of the mechanism control computer
(Note : For details, see the specifications of the mechanism control computer.)

(13) Disc sensing
The type of discs loaded is displayed
: [DVD], [CD], [CDV], [LD], [VCD], [ ]

(14) Pickup (PU–***]
The pickup being operating is displayed:
DVDs : [DVD]
CLDs : [CLD]

(15) Revision setting for the player [REGION : *]
Setting numbers : [1]–[8]

(16) Version of the FL control computer
Destination setting : [F : ****/*]
Four characters in front represent the type of model :
Base : Base model
Omni : Compatible model
B/FX : Base FX
O_KR : Compatible Karaoke
B_OM : Base OEM
O_OM : Compatible OEM
Two characters that follow represent the destination code:
J : /J, U : /KU, C : /KC, S : SL, W : WY,
K : KU/KC, E : Elite
Version No. : [F : *.*]

(17) Version of the system control computer
Parts number (PD*****) : [S : *****]
Version No. : [S : *.**]

(18) Version of the DVD mechanism control computer
Parts number (PD******) : [M : ******]
Revision No. : [M : *.***]

(19) Version of the CLD mechanism control computer
Parts number (PD******) : [L : ******]
Revision No. : [L : *.***]

5. IC INFORMATION

• The information in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

● List of IC

PD4753B	HM514800CJ-7	UPD4516161G5-A12-7JF	BA6797FP
PD0246A2	PD4784A	PD4696A	CXA2521AQ
PD0236AM	ZR38521	PA0065AM	MBM29F400TA-70PF
HD6417032F20	UPD61021	TLC5540INS	
PD4695A	IR3C07N	CXD2545Q	

■ PD4753B [DV-500 : (FLKB ASSY : IC101)]
[DVL-90, DVL-700 : (FLPB ASSY : IC101)]

● MODE CONTROL IC

● Pin Function

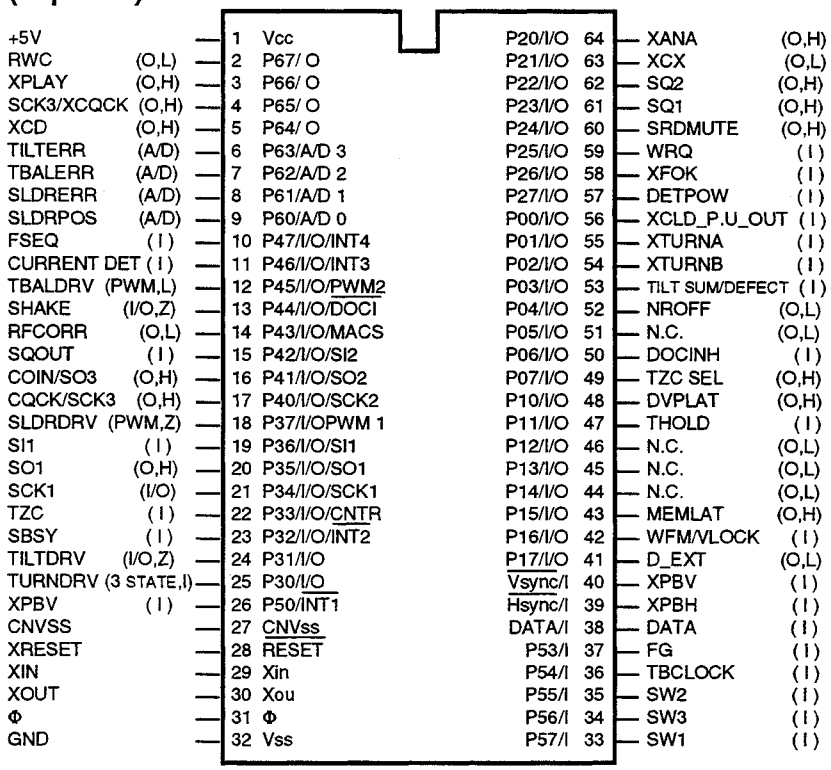
No.	Name	Function Name	I/O	Function	ACTIVE
1	P94	T6	O	FL timing output.	H : ON
2	P93	T5	O		
3	P92	T4	O		
4	P91	T3	O		
5	P90	T2	O		
6	P81	T1	O		
7	P80	T0	O		
8	V_{DD}	Vcc	–	–	–
9	P27	Angle LED	O	Angle LED ON/OFF.	H : ON
10	P26	SIDE A LED	O	SIDE A LED ON/OFF. Basically (NC) only with compatible.	H : ON
11	P25	SIDE B LED	O	SIDE B LED ON/OFF. Basically (NC) only with compatible.	H : ON
12	P24	DVD illumination	O	DVD illumination lamp ON/OFF.	H : ON
13	P23	XRDY	O	Communications handshake line with system controller.	L: communications enabled
14	P22	SCK1	I/O	Communication clock output with system controller.	–
15	P21	SO1	I/O	Communication data output with system controller.	–
16	P20	SI1	I	Communication data input with system controller.	–
17	$\overline{RESET}$	RESET IN	I	Reset input.	L: reset
18	P74	Condition LED	O	Condition OED ON/OFF.	L : ON
19	P73	Last memory LED	O	Last memory LED ON/OFF.	L : ON
20	AVss	Vss	–	–	–
21	P17	POWER ON	O	SW5V ON/OFF.	H : ON
22	P16	RESET OUT	O	System reset output.	L: reset
23	P15	(NC)	O	–	–
24	P14	(NC)	O	–	–
25	P13	KIN1	I	Key input.	
26	P12	KIN0	I	Key input.	
27	P11	MS1	I	Destination determination input.	
28	P10	MS0	I	Destination determination input.	
29	AV_{DD}	AV_{DD}	–	–	–
30	AVREF	AVREF	–	–	–

No.	Name	Function Name	I/O	Function	ACTIVE
31	P04	P04	I	(Not used)	–
32	XT2	(NC)	–	–	–
33	Vss	Vss	I	–	–
34	X1	X1	I	Microprocessor clock connection.	
35	X2	X2	–	Microprocessor clock connection.	
36	P37	(NC)	O		
37	P36	(NC)	O		
38	P35	(NC)	O	–	–
39	P34	(NC)	O		
40	P33	(NC)	O		
41	P32	(NC)	O		
42	P31	(NC)	O		
43	P30	(NC)	O	–	–
44	P03	(NC)	O		
45	P02	(NC)	O		
46	P01	LT1	I	Communications handshake line with system controller.	L: communications enabled
47	P00	SEL IR	I	Remote control signal input.	
48	IC	IC	–	–	–
49	P72	(NC)	O		
50	P71	(NC)	O	–	–
51	P70	(NC)	O		
52	VDD	VDD	–	–	–
53	P127	DISP LED	O	Display LED ON/OFF.	H : ON
54	P126	GUI LED	O	GUI LED ON/OFF.	H : ON
55	P125	(NC)	O		
56	P124	(NC)	O	–	–
57	P123	(NC)	O		
58	P122	S15	O		
59	P121	S14	O		
60	P120	S13	O	FL segment output.	H : ON
61	P117	S12	O		
62	P116	S11	O		
63	P115	S10	O		
64	P114	(NC)	O	–	–
65	P113	(NC)	O		
66	P112	S9	O		
67	P111	S8	O		
68	P110	S7	O	FL segment output.	H : ON
69	P107	S6	O		
70	P106	S5	O		
71	VLOAD	-30V	–	Input for -30V.	
72	P105	S4	O		
73	P104	S3	O		
74	P103	S2	O	FL segment output.	H : ON
75	P102	S1	O		
76	P101	S0	O		
77	P100	T10	O		
78	P97	T9	O	FL segment output.	H : ON
79	P96	T8	O		
80	P95	T7	O		

■ PD0246A2 (CLD MAIN ASSY : IC101)(DVL-90, DVL-700 ONLY)

● LD MECHANISM CONTROL IC

● Pin Arrangement (Top View)



● Pin Function

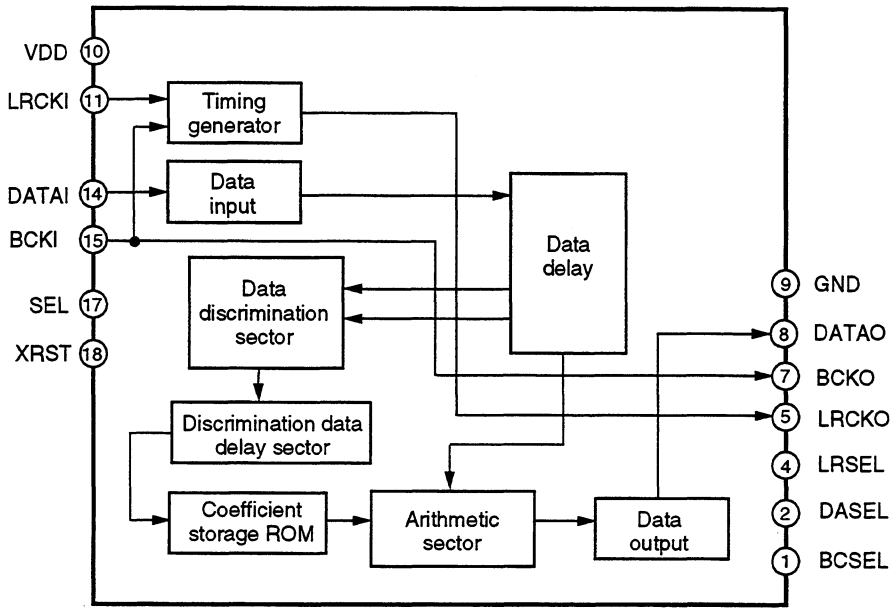
No.	Pin Name	I/O	Pin Function
1	VCC	I	Power supply pin Apply 5V ± 10%
2	RWC	O	DSP read/write command signal output "L"= Read "H"= Write
3	XPLAY	O	Signal output during spindle servo "L"= During servo "H"= During acceleration, brake and stop
4	SCK3/XCQCK	O	DVP/DSP clock switch "H"= DVP "L"= DSP
5	XCD	O	LD/CD switch signal output "L= CD "H"= LD
6	TILTERR	I A/D	This signal is A/D converted as the tilt servo control input. Control the tilt motor so that this signal becomes 2.5V.
7	TBALERR	I A/D	Tracking balance error signal input This signal is A/D converted as the tracking offset control input.
8	SLDERR	I A/D	This signal is A/D converted as the slider servo control input. Control the slider motor so that this signal becomes 2.5V.
9	SLDPOS	I A/D	Pickup position detection switch input Detect the position by reading A/D input value which each switches are resistance divided.
10	FSEQ	I	Subcode sync. confirmity detection signal input "L"= Not confirmity "H"= Confirmity
11	CURRENTDET	I	Spindle over-current detection signal input "L" = Over current "H"= Normal
12	TBALDRV	O PWM	Output the tracking offset signal to PWM output, then use for auto tracking offset. 910μsec period, tri-state control H, L, Z
13	SHAKE	I/O	Handshake signal for data communication with the mode control IC This pin is the bilateral data line and each microprocessor control the Input/Output.
14	RFCORR	O	RF correction switch signal output "H"= Gain UP CD, CDV-A:Low, CAV inner circuit gain up, others are High.
15	SQOUT	I	Command data input from DSP Read out SUBQ
16	SO3/COIN	O	Command data output to DVP/DSP
17	SCK3/CQCK	O	DVP/DSP read/write command clock output Read-in at rising edge
18	SLDDRV	O PWM	Slider control signal output 5V= FWD, 0V= REV, 2.5V= STOP 910μsec period, tri-state control H, L, Z

No.	Pin Name	I/O	Pin Function
19	SI1	I	Data input from the mode control IC
20	SO1	O	Serial data output to the mode control IC
21	SCK1	I/O	Clock for serial communication with the mode control IC Becomes input mode without communicate with the mode control IC
22	TZC	I INT	Tracking error zero cross signal input Monitor this signal when searching track count in the miss clamp detection
23	SBSY	I	Subcode block sync. input
24	TILTDRV	I/O	LOAD/TILT control output 0.5V= Tray IN, OUT/Tilt DOWN, UP 2.5V=STOP Use for tilt servo that tilt drive is PWM output.
25	TURNDRV	O	Turn drive signal output
26	XPBV	I	Playback vertical sync. signal input of LD/CDV "L"= During vertical sync.
27	CNVSS	I	Ground for A/D conversion
28	XRESET	I	Reset signal input "L"= Reset "H"= Release reset Mode control IC is controlled.
29	XIN	I	9MHz clock oscillation input
30	XOUT	O	9MHz clock oscillation output
31	N.C.	O	Not used
32	GND	I	Ground
33	SW1	I	Switch input for Loading/Tilt position detection
34	SW3		
35	SW2		
36	TBCLOCK	I	Spindle lock signal input "L"= Unlock "H"= Lock
37	FG	I	Spindle motor FG signal input 16 outputs per rotation Used after dividing by 2 in the microprocessor
38	DATA	I	Input for Phillips code decoder with built-in mechanism controller
39	XPBH	I	Playback H-SYNC input for Phillips code decoder
40	XPBV	I	Playback V-SYNC input for Phillips code decoder
41	D_EXT	O	Control signal output for video dynamic extension "H"= ON "L"= OFF
42	WFM	I	Field discrimination signal from DVP "H"= ODD "L"= EVEN
43	MEMLAT	O	Serial control latch output of memory control IC PD3212A Latches at falling edge.
44	N.C.	O	Not used
45	N.C.	O	Not used
46	N.C.	O	Not used
47	THOLD	I	Track jump accelerating / decelerating signal input "L"= Other "H"= During accelerating / decelerating
48	DVPLAT	O	PD6159B serial latch signal output Latches at falling edge.
49	TZCSEL	O	TZC switch signal output "H"= at normal "L"= at CD/DVD disc discrimination
50	DOCINH	O	Control the clamp pulse and clamp killer by tri-state value
51	N.C.	O	Not used
52	NROFF	O	Noise reduction control output by VDEM "L"= Normal "H"= Not NR
53	TILT SUM	O	Disc present/absent detecting signal input by the tilt sum in the DVD P.U. mode "H"= Absent "L"= Present
54	XTURNB	I	Turn switch input "H"= Side A / turn "L"= Side B
55	XTURNA	I	Turn switch input "H"= Side B / turn "L"= Side A
56	XLDPUCUT	I	LD P.U. out position detecting switch input "H"= LD P.U. active "L"= LD P.U. out position
57	DETPOW	I	Use for power abnormal signal input port "L"= Normal "H"= Abnormal
58	XFOK	I	Focus servo lock signal input "L"= Lock "H"= Unlock Use for lock detection of focus servo
59	WRQ	I	Subcode Q reading OK signal input "L"= NG "H"= OK This pin will be H when subcode Q data passed by CRC check.
60	SRDMUTE	O	Mute control signal output for AC3 Release MUTE during playback. "L"= Release MUTE "H"= MUTE
61	SQ1	O	Analog audio switching signal output 1/L "L"= Squelch OFF "H"= Squelch ON
62	SQ2	O	Analog audio switching signal output 2/R "L"= Squelch OFF "H"= Squelch ON
63	XCX	O	Analog audio CX noise reduction switching signal output "L"= CX ON "H"= CX OFF
64	XANA	O	Digital / Analog audio switching signal output "L"= Analog "H"= Digital

■ PD0236AM [DV-500 : (AUDB ASSY : IC102)]
[DVL-90, DVL-700 : (CLD MAIN ASSY : IC202)]

● HI-BIT IC

● Block Diagram



● Pin Function

No.	Pin Name	I/O	Pin Function
1	BCSEL	Ip	fs selection of bit clock (built-in pull-up) H : BCKI = 48fs , L : BCKI = 64fs
2	DASEL	Ip	Output data length selection when the bit length expansion function is ON. H :DATAO = 20 bit , L : DATAO = 24 bit
3	(NC)	–	Not used (Open or VDD)
4	LRSEL	Ip	LRCKO polarity selection (built-in pull-up) H : LRCKI = LRCKO , L : LRCKI = $\overline{\text{LRCKO}}$
5	LRCKO	O	LR clock output
6	(NC)	–	Not used (Open or VDD)
7	BCKO	O	Bit clock output
8	DATAO	O	Data output
9	GND	–	Ground pin
10	VDD	–	Power supply pin
11	LRCKI	I	LR clock input
12	(NC)	–	Not used (Open or VDD)
13	(NC)	–	Not used (Open or VDD)
14	DATAI	I	Data input
15	BCKI	I	Bit clock input
16	(NC)	–	Not used (Open or VDD)
17	SEL	Ip	Bit length expansion process / input data output selection (built-in pull-up) H :Expansion process (output word length : 20/24 bit), L : Input data output
18	XRST	I	Reset pin H : Normal , L : Reset

■ HD6417032F20 (DVD MAIN ASSY : IC101)

● SYSTEM μ- COM

● Pin Function

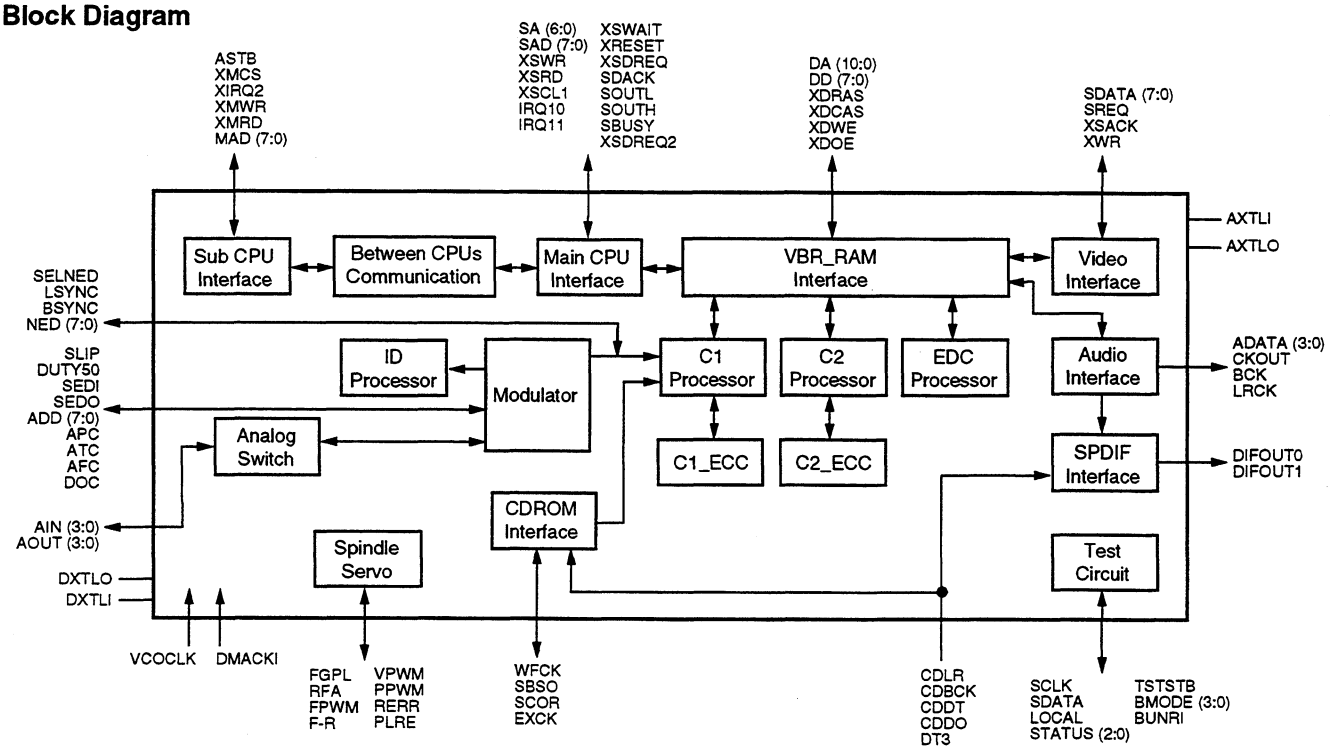
No.	Name	Signal Name	I/O	Active	Function
1	XIRQ6	XIRQ6	I	L	Interrupt input from LSI-1.
2	XIRQ7	XIRQ7	I	L	Interrupt input from μPD61020.
3	Vss	Vss	-	-	Grounding.
4	AD0	AD0	I/O	-	Data bus.
5	AD1	AD1	I/O	-	
6	AD2	AD2	I/O	-	
7	AD3	AD3	I/O	-	
8	AD4	AD4	I/O	-	
9	AD5	AD5	I/O	-	
10	AD6	AD6	I/O	-	
11	AD7	AD7	I/O	-	
12	Vss	Vss	-	-	Grounding.
13	AD8	AD8	I/O	-	Data bus.
14	AD9	AD9	I/O	-	Data bus.
15	Vcc	Vcc	-	-	Power supply.
16	AD10	AD10	I/O	-	Data bus.
17	AD11	AD11	I/O	-	
18	AD12	AD12	I/O	-	
19	AD13	AD13	I/O	-	
20	AD14	AD14	I/O	-	
21	AD15	AD15	I/O	-	
22	Vss	Vss	-	-	Grounding.
23	A0 (XHBS)	A0 (XHBS)	O	-	
24	A1	A1	O	-	
25	A2	A2	O	-	
26	A3	A3	O	-	Address bus.
27	A4	A4	O	-	
28	A5	A5	O	-	
29	A6	A6	O	-	
30	A7	A7	O	-	
31	Vss	Vss	-	-	Grounding.
32	A8	A8	O	-	Address bus.
33	A9	A9	O	-	
34	A10	A10	O	-	
35	A11	A11	O	-	
36	A12	A12	O	-	
37	A13	A13	O	-	
38	A14	A14	O	-	
39	A15	A15	O	-	
40	Vss	Vss	-	-	Grounding.
41	A16	A16	O	-	Address bus.
42	A17	A17	O	-	Address bus.
43	Vcc	Vcc	-	-	Power supply.
44	A18	A18	O	-	Address bus.
45	A19	A19	O	-	
46	A20	A20	O	-	
47	A21	A21	O	-	
48	XCS0	XCS0	O	L	Chip selection to program ROM.
49	XCS1	XCS1	O	L	Chip selection to work SRAM.
50	XCS2	XCS2	O	L	Chip selection to GUI-ROM.
51	XCS3	XCS3	O	L	Chip selection to LSI-1.
52	Vss	Vss	-	-	Grounding.
53	XCS4	XCS4	O	L	Chip selection to LSI-2.
54	XCS5	XCS5	-	-	Not used.
55	XCS6	XCS6	O	L	Chip selection to μPD61020.
56	XWAIT	XWAIT	I	L	Weight input for bus cycle.

No.	Name	Signal Name	I/O	Active	Function
57	XWR	XWR	O	L	Signal for external write.
58	PA5	PA5	O	-	TP58 (test pin).
59	XRD	XRD	O	L	Signal for external read.
60	PA7	XLT3	O	L	Latch signal to PD2026/29.
61	Vss	Vss	-	-	Grounding.
62	PA8	XLT2	O	L	Latch signal to ZR38521.
63	PA9	XDAKE	O	L	LSI-1 and LSI-2 direct DMA enable output.
64	TIOCA1	XQ2	I	L	Interrupt input from LSI-2.
65	PA11	LT1	O	H	Handshake output to FL CON.
66	DACK0	DACK0	O	H	Signal to acknowledge request for DMA transfer to LSI-1.
67	XDREQ0	XDREQ0	I	L	Signal to acknowledge request for DMA transfer from LSI-1.
68	DACK1	DACK1	O	L	Signal to acknowledge request for DMA transfer to LSI-2.
69	XDREQ1	XDREQ1	I	L	Signal to acknowledge request for DMA transfer from LSI-2.
70	Vcc	Vcc	-	-	Power supply.
71	CK	CK	O	-	System control clock output. Not used.
72	Vss	Vss	-	-	Grounding.
73	EXTAL	EXTAL	I	-	Crystal oscillator input.
74	XTAL	XTAL	I	-	Crystal oscillator input.
75	Vcc	Vcc	-	-	Power supply.
76	NMI	NMI	I	-	NMI input (pull-up). Not used.
77	Vcc	Vcc	-	-	Power supply.
78	XWDTOF	WDTOF	O	L	Watchdog timer output. Not used.
79	XRES	XRES	I	L	Reset input.
80	MD0	MD0	I	-	Operation mode setting terminal (H).
81	MD1	MD1	I	-	Operation mode setting terminal (L). Set to Mode 1.
82	MD2	MD2	I	-	Operation mode setting terminal (L).
83	Vcc	Vcc	-	-	Power supply.
84	Vcc	Vcc	-	-	Power supply.
85	AVcc	AVcc	I	-	Analog power supply.
86	AVref	AVref	-	-	Analog reference voltage input.
87	AN0	AN0	-	-	Analog signal input (pull-up). Not used.
88	AN1	AN1	I	-	Analog signal input (pull-up). Not used.
89	AN2	AN2	I	-	Audio level (Lch) input.
90	AN3	AN3	I	-	Audio level (Rch) input.
91	AVss	AVss	-	-	Analog power grounding.
92	PC4	XSDET	I	-	Sync detection input.
93	PC5	XSEL2	I	-	Test mode determination input.
94	PC6	CDGM	I	H	Graphic input data detection input.
95	PC7	CTS	I	H	CTS (for RS-232).
96	Vss	Vss	-	-	Grounding.
97	PB0	FMATT	O	-	LD FM audio attenuation output.
98	PB1	BSEL	O	-	Hi Bit clock selection output.
99	Vcc	Vcc	-	-	Power supply.
100	TIOCA3	HIBSEL	O	-	Hi Bit expansion selection output.
101	PB3	XIRQCDROM	I	-	Interrupt input from CDROM decoder.
102	PB4	XRDY	I	L	Ready signal input from FL microprocessor.
103	PB5	DTR	O	-	DTR output (for RS-232).
104	PB6	GCS	O	H	Chip selection for CDG.
105	PB7	DPSEL	O	-	Optical output selection output. $\overline{\text{PCM}}$/AC3.
106	Vss	Vss	-	-	Grounding.
107	RxD0	SSI	I	-	Serial IN (synchronizing the clock).
108	TxD0	SSO	O	-	Serial OUT (synchronizing the clock).
109	RxD1	RXD	I	-	Serial IN (synchronizing adjustment).
110	TxD1	TXD	O	-	Serial OUT (synchronizing adjustment).
111	SCK0	SSCK	I/O	-	Serial clock input/output (synchronizing the clock).
112	XIRQ5	XQ10	I	L	Interrupt input from LSI-1 INT1.

■ PD4695A (DVD MAIN ASSY : IC161)

● DVD DECODER

● Block Diagram



● Pin Function

No.	Pin Name	I/O	Pin Function
1	GND	–	Ground for digital circuit
2	GND		
3	DXTLO	O	Connect a 27MHz crystal which is oscillated PLL reference clock
4	DXTLI	I	When input a signal from the external, connect to DXTLI.
5	VDD	–	Power supply for digital circuit Connect to +5V.
6	PEQL	I	Not used Fixed to GND or VDD.
7	PEQH	I	
8	SELNED	I	Set the input/output direction of NED (7:0), STB and BSYNC pins 0 for input.
9	STB	I/O	Strobe signal which is indicated data of after the 8/16 demodulation is in NED (7:0) pins
10	BSYNC	I/O	Pulse which is indicated the lead of ECC block
11	NED7	I/O	8 bit parallel data input/output of after the 8/16 demodulation
12	NED6		
13	NED5		
14	NED4		
15	VDD	–	Power supply for digital circuit Connect to +5V.
16	GND	–	Ground for digital circuit
17	NED3	I/O	8 bit parallel data input/output of after the 8/16 demodulation
18	NED2		
19	NED1		
20	NED0		
21	DD7	I/O	DRAM data bus for VBR buffer
22	DD6		
23	DD5		
24	DD4		
25	DD3		
26	GND	–	Ground for digital circuit

No.	Pin Name	I/O	Pin Function
27	VDD	–	Power supply for digital circuit Connect to +5V.
28	DD2	I/O	DRAM data bus for VBR buffer
29	DD1		
30	DD0		
31	XDCAS	O	DRAM CAS signal of VBR buffer
32	XDWE	O	DRAM WE signal of VBR buffer
33	XDOE	O	DRAM OE signal of VBR buffer
34	XDRAS	O	DRAM RAS signal of VBR buffer
35	DA10	O	DRAM address signal for VBR buffer
36	DA9		
37	DA8		
38	DA7		
39	DA6		
40	GND	–	Ground for digital circuit
41	VDD	–	Power supply for digital circuit Connect to +5V.
42	DA5	O	DRAM address signal for VBR buffer
43	DA4		
44	DA3		
45	DA2		
46	DA1		
47	DA0		
48	SREQ	I	Data transfer request pin from the MPEG decoder
49	XWR	O	Data transfer response pin to the MPEG decoder Output form is changed by setting.
50	XSACK		
51	GND	–	Ground for digital circuit
52	GND		
53	VDD	–	Power supply for digital circuit Connect to +5V.
54	SDATA0	O	Data output bus to the MPEG decoder
55	SDATA1		
56	SDATA2		
57	SDATA3		
58	GND	–	Ground for digital circuit
59	VDD	–	Power supply for digital circuit Connect to +5V.
60	SDATA4	O	Data output bus to the MPEG decoder
61	SDATA5		
62	SDATA6		
63	SDATA7		
64	LSYNC	O	Line sync. detecting output in the demodulator
65	DMACKI	I	System clock input of DVD and CD ROM decoder Input 10 to 29MHz.
66	GND	–	Ground for digital circuit
67	DMCKO	O	Outputs a clock which is oscillated and input at DXTLI and DXTLO pins Normally, connect to DMACKI.
68	XSCL1	I	Chip select signal from the main CPU When this signal is Low, XSRD/XSWR becomes effectively.
69	XSWAIT	O	WAIT output against to the main CPU When this pin is Low, you should not stop the access from the main CPU. This pin is open-drain.
70	XSRD	I	Connect to RD signal of main CPU
71	XSWR	I	Connect to WR signal of main CPU
72	XSDREQ	O	DMA request against to the main CPU Drive the DMA transfer at Low level or falling edge.
73	SDACK	I	DMA response signal When this signal is High, outputs the data to SAD (7:0).
74	XSDREQ2	I	Connect the DMA request signal of other device.
75	SA6	I	Connect the address bus of the main CPU
76	SA5		
77	SA4		

No.	Pin Name	I/O	Pin Function
78	VDD	–	Power supply for digital circuit Connedct to +5V.
79	GND	–	Ground for digital circuit
80	SA3	I	Connect the address bus of the main CPU
81	SA2		
82	SA1		
83	SA0		
84	SOUTH	O	Serial output which is used the DMA channel of CPU Outputs the upper nibble.
85	SAD7	I/O	Connect the data bus of the main CPU
86	SAD6		
87	SAD5		
88	SAD4		
89	VDD	–	Power supply for digital circuit Connedct to +5V.
90	GND	–	Ground for digital circuit
91	SAD3	I/O	Connect the data bus of the main CPU
92	SAD2		
93	SAD1		
94	SAD0		
95	DUTY50	O	Always outputs the duty 50% pulse Apply the reference voltage of each PWM signal of demodulation system.
96	XIRQ10	O	Low for require the interrupt against to the main CPU Setable the output pins with the register.
97	XIRQ11		
98	TSTSTB	I	Set the LSI to operate the test mode Test mode for High input.
99	BMODE0	I	Set to perform the any test in the test mode
100	BMODE1		
101	BMODE2		
102	BMODE3		
103	BUNRI	I	Separation test control pin of the internal RAM Inputs Low in the actual use.
104	VDD	–	Power supply for digital circuit Connedct to +5V.
105	GND	–	Ground for digital circuit
106	GND		
107	AXTLO	O	36.864MHz or 24.576MHz crystal connect pin which is oscillated the reference clock to use the audio output circuit.
108	AXTLI	I	When input a signal from the external, connect to AXTLI.
109	VDD	–	Power supply for digital circuit Connedct to +5V.
110	CKCD	I	Reference clock of CD audio output Inputs 16.9MHz.
111	GND	–	Ground for digital circuit
112	PV	O	When the master clock is AV synchronized, outputs the pulse which is frequency divided the audio side clock (AXTLI input) for apply to the PLL circuit.
113	PREF	O	When the master clock is AV synchronized, outputs the pulse which is frequency divided the video side clock (DMACKI input) for apply to the PLL circuit.
114	CKOUT	O	Frequency divided signal which is connected to AXTL pin and use for DAC control Frequency is changed by the mode.
115	BCK	O	Bit clock output to DAC and audio decoder It is 48fs or 64fs of the source.
116	LRCK	O	LRCK signal output to DAC and audio decoder
117	ADATA0	O	Outputs the compression data when source is AC3/MPEG and outputs CH0/CH1 when source is linear.
118	ADATA1	O	Output CH2/CH3 when source is linear
119	ADATA2		
120	ADATA3		
121	SBUSY	I	Busy signal for output control the serial output of SOUTL, SOUTH pins
122	DIFOUT0	O	Digital output by switching the compression data and linear data When linear data is output, output the same as that of the DIFOUT1.
123	DIFOUT1	O	Digital out for linear data only Outputs CH0&CH1/AC3/MPEG/CD of DVD linear correspond to the source.
124	VALID	O	When source is AC3/MPEG, it becomes High level during effective data output
125	DT3	I	Inputs linear data after the decode from audio decoder This data is digital output. Audio data is slave movement.

No.	Pin Name	I/O	Pin Function
126	CDBCK	I	Bit clock input from the CD decoder Expect frequency is 2.1168MHz (48fs).
127	CDLR	I	LRCK signal input from the CD decoder
128	CDDT	I	Audio data input from the CD decoder
129	CDDO	I	Digital output signal input from the CD decoder Outputs by switching it of DVD into LSI.
130	VDD	–	Power supply for digital circuit Connect to +5V.
131	GND	–	Ground for digital circuit
132	WFCK	I	CD frame clock signal Connect to same pin name pin of the CD decoder IC.
133	SCOR	I	CD subcode sync. input Connect to same pin name pin of the CD decoder IC.
134	SBSO	I	CD subcode data input Connect to same pin name pin of the CD decoder IC.
135	EXCK	O	Shift clock to making the timing of data transfer to SBSO pin
136	SOUTL	O	Serial output which is used the DMA channel of CPU and outputs the lower nibble
137	ASTB	I	Strobe signal which is indicated the address information in MAD (7:0) Connect to ASTB of sub CPU.
138	XMCS	I	Chip select signal from the sub CPU When this signal is Low, XMRD/XMWR will be effective.
139	XIRQ2	I	Low for require the interrupt against to the sub CPU
140	XMWR	I	Connect to WR signal of the sub CPU
141	XMRD	I	Connect to RD signal of the sub CPU
142	MAD7	I/O	Connect to multiplex bus of address data of the sub CPU
143	MAD6		
144	MAD5		
145	MAD4		
146	VDD	–	Power supply for digital circuit Connect to +5V.
147	GND	–	Ground for digital circuit
148	MAD3	I/O	Connect to multiplex bus of address data of the sub CPU
149	MAD2		
150	MAD1		
151	MAD0		
152			
153			
154			
155	GND	–	Ground for digital circuit
156	GND		
157	VDD	–	Power supply for digital circuit Connect to +5V.
158	XRESET	I	Initialize the whole LSI system by Low level input
159	FGPL	I	Rotation pulse input from the spindle motor
160	RFA	I	External binary RF signal input for the rough servo Connect to GND at not used.
161	FPWM	O	7 bit PWM output for the FG servo Tri-state output of High, Low and Hi-impedance
162	F_R	O	Rotaion direction of the spindle motor indicating output
163	VPWM	O	5 bit PWM output for the velocity servo Tri-state output of High, Low and Hi-impedance
164	GND	–	Ground for digital circuit
165	VDD	–	Power supply for digital circuit Connect to +5V.
166	PPWM	O	PWM output for the phase servo Tri-state output of High, Low and Hi-impedance
167	RPWM	O	4 bit PWM output for the rough servo Tri-state output of High, Low and Hi-impedance
168	RERR	O	Control pin for the rough servo Tri-state output of High, Low and Hi-impedance
169	PLRE	O	RRPW pin output without tri-state control
170	LOCAL	I	Input for local operaion of the demodulation system
171	SCLK	O	Clock pulse output with synchronizing the main data after the 8/16 demodulation Test signal to connect the error measuring instrument
172	SDATA	O	Serial output the main data after the 8/16 demodulation Test signal to connect the error measuring instrument
173	SEDI	I	Serial data input after the viterbi decoding Normally, connect to SEDO pin.
174	SEDO	O	Serial data output after the viterbi decoding Normally, connect to SEDI pin.
175	GND	–	Ground for digital circuit

No.	Pin Name	I/O	Pin Function
176	VCOCLK	I	System clock of the spindle demodulator Connect to the external VCO.
177	SLIP	O	When PLL cycle slip is occured, outputs the pulse of prescribed width.
178	APC	O	Phase difference of PLL outputs as PWM pulse
179	ATC	O	DC difference of RF signal outputs as PWM pulse
180	AFC	O	Frequency difference of PLL outputs as PWM pulse
181	DOC	O	When the polarity of RF signal is not turned more than 32 clocks, it is supposed to drop out then output the flag.
182	GND	–	Ground for digital circuit
183	VDD	–	Power supply for digital circuit Connect to +5V.
184			
185	AVDD	–	Power supply for analog circuit Connect to +5V.
186	AIN0	I	Analog switch input/output for controling the amplitude of RF signal
187	AOUT0	O	Analog switch is ON/OFF correspond to the amplitude of RF signal
188			
189	AIN1	I	Analog switch input/output for controling the amplitude of RF signal
190	AOUT1	O	Analog switch is ON/OFF correspond to the amplitude of RF signal
191			
192			
193	AIN2	I	Analog switch input/output for controling the amplitude of RF signal
194	AOUT2	O	Analog switch is ON/OFF correspond to the amplitude of RF signal
195			
196			
197	AIN3	I	Analog switch input/output for controling the amplitude of RF signal
198	AOUT3	O	Analog switch is ON/OFF correspond to the amplitude of RF signal
199	AGND	–	Ground for analog circuit
200	ADD0	I	Input RF sampling value after the A/D conversion to 8 bit parallel data
201	ADD1		
202	ADD2		
203	ADD3		
204	ADD4		
205	ADD5		
206	ADD6		
207	ADD7		
208	VDD	–	Power supply for digital circuit Connect to +5V.

■ HM514800CJ-7 (DVD MAIN ASSY : IC162)

● 4M DRAM

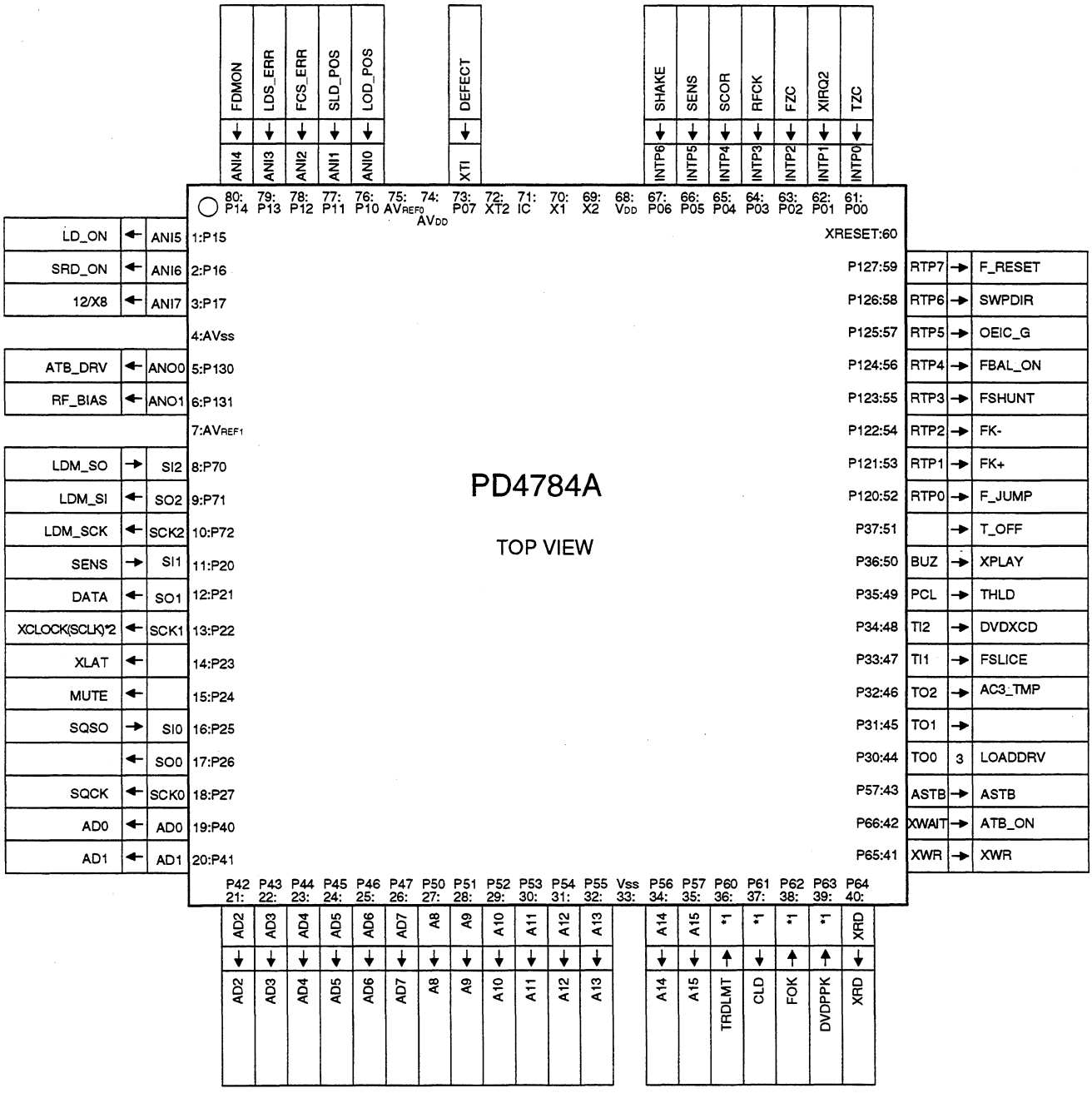
● Pin Function

No.	Pin Name	Pin Function
1	Vcc	Power supply
2	I/O0	Data input/output
3	I/O1	
4	I/O2	
5	I/O3	
6	NC	Non connection
7	$\overline{WE}$	Read/Write enable
8	$\overline{RAS}$	Low address strobe
9	A9	Address input/Refresh address input
10	A0	
11	A1	
12	A2	
13	A3	
14	Vcc	Power supply
15	Vss	Ground
16	A4	Address input/Refresh address input
17	A5	
18	A6	
19	A7	
20	A8	
21	NC	Non connection
22	OE	Output enable
23	CAS	Column address strobe
24	I/O4	Data input/output
25	I/O5	
26	I/O6	
27	I/O7	
28	Vss	Ground

■ PD4784A (DVD MAIN ASSY : IC201)

● MECHANISM CONTROL IC

● Pin Assignment



*1 Sets to open drain output during output.

*2 Connect to the XCLOC and SCLK terminals of CXD2545Q.

● Pin Function

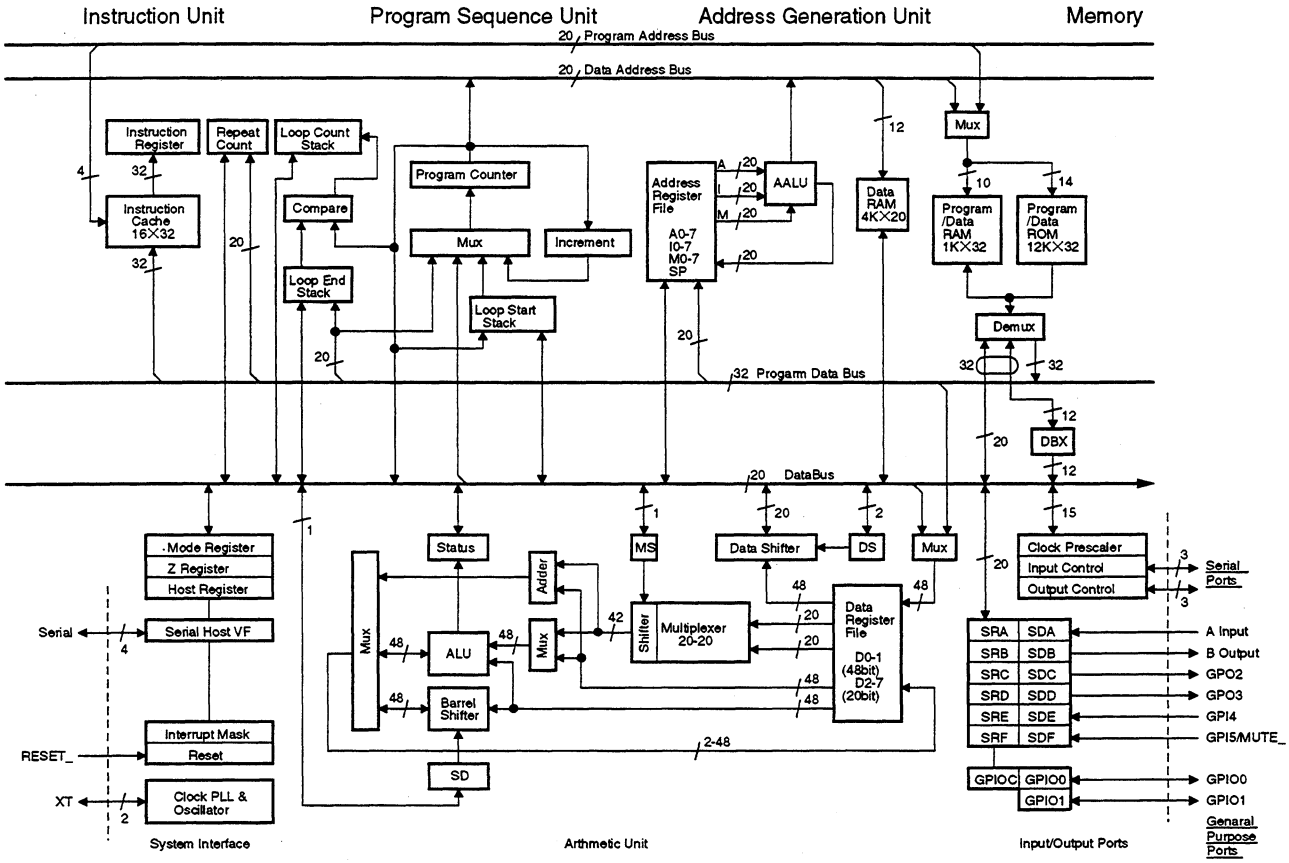
No.	Name	I/O	Function
1	LD_ON	OUT	Laser diode ON signal. H: active
2	SRD_ON	OUT	Switches command clock inhibit during serial read out. H: inhibit
3	12/X8.	OUT	DVD 8/12 cm switching signal.
4	AVss	-	Analog Ground.
5	ATB_DRV	D/A	ATB drive.
6	RF_BIAS	D/A	RD BIAS drive.
7	AVref1	-	Analog Reference Voltage1.
8	LDM_SO	Serial I	LD mechanical controller communications data IN (SD ← LD).
9	LDM_SI	Serial O	LD mechanical controller communications data OUT (SD → LD).
10	LDM_SCK	Serial O	LD mechanical controller communications data CLOCK (SD ← LD).
11	SENS	Serial I	CXD2545Q Serial Read Out function output data input.
12	DATA	Serial O	CXD2545Q command data output.
13	XCLOCK (SCLK)	Serial O	Clock for CXD2545Q command/serial read out function.
14	XLAT	OUT	CXD2545Q LATCH signal.
15	MUTE	OUT	Power ON MUTE signal.
16	SQSO	Serial I	CXD2545Q SubQ data input.
17	NC.	OUT	Available.
18	SQSK	Serial O	Clock for CXD2545Q SubQ.
19	AD0	IO	Address/Data Bus.
20	AD1	IO	
21	AD2	IO	
22	AD3	IO	
23	AD4	IO	
24	AD5	IO	
25	AD6	IO	
26	AD7	IO	
27	A8	OUT	Address Bus.
28	A9	OUT	
29	A10	OUT	
30	A11	OUT	
31	A12	OUT	
32	A13	OUT	
33	Vss	-	Ground.
34	A14	Expansion IO	Address Bus.
35	A15	Expansion IO	Address Bus.
36	TRDLMT.	IN	Tracking drive limit current detection signal input.
37	CLD	IN	Signal to control whether the pick of DVD or CD is active (Used with CLD compatible.).
38	FOK	IN	Focus OK signal.
39	DVDPRK	IN	DVD slider park IN signal (Used with CLD compatible.).
40	XRD	OUT	Read Strobe.

No.	Name	I/O	Function
41	XWR	OUT	Write Strobe.
42	ATB_ON	OUT	For ATB circuit ON/OFF.
43	ASTB	OUT	Address Strobe.
44	LOAD DRV	OUT	Loading drive.
45	NC.	OUT	Available.
46	AC3_TMP.	OUT	Signal for controlling AC3.
47	NC.	OUT	Available.
48	DVD/XCD	OUT	DVD/CD change-over SW (H: DVD, L: CD). The switch switches spindle error signal, etc.
49	THLD	OUT	Tracking hold signal ("H" duing jump).
50	XPLAY	OUT	For off-track measure circuit.
51	T_OFF		
52	F_JUMP	OUT	Focus jump switching signal ("H" during jump).
53	FK+	OUT	Focus jump kick pulse (+).
54	FK-	OUT	Focus jump kick pulse (-).
55	FCHUNT	OUT	Focus SHUNT SW control.
56	FBAL_ON	OUT	Focus Balance circuit control signal.
57	OEIC_G	OUT	OEIC GAIN SW switching signal.
58	SWPDIR	OUT	Sweep direction control.
59	GAIN_JDGE	OUT	Signal for disc judgment.
59	F_RESET	OUT	Peak hold reset signal for focus S.
60	XRESET	-	Mechanical controller hardware reset signal.
61	TZC	IN	TZC input.
62	XIRQ	IN	LSI1 interrupt (DVD-ID, system controller communications, FG-spindle).
63	FZC	IN	FZC interrupt (focus jump).
64	RFCK	IN	RFCK interrupt (error rate measurement).
65	SCOR	IN	SCOR interrupt (SubQ).
66	SENS	IN	SENS interrupt (fine search/MTJ) SENS monitor.
67	SHAKE	I/O	SHAKE interrupt input/SHAKE output (LD mechanical controller communications when CLD compatible is used).
68	Vdd	-	Power Supply (+5V).
69	X2	-	Cristal (Main System Clock).
70	X1	-	Cristal (Main System Clock).
71	IC	-	Internally Connected.
72	XT2	-	Crystal (Sub System Clock) ← Clock.
73	DEFECT	IN	DETECT signal input.
74	AVdd	-	Analog Power Supply.
75	AVref0	-	Analog Refernce Voltage0.
76	LOAD_POS	A/D	Loading SW read signal.
77	SLD_POS	A/D	Slider SW read signal.
78	FCS_ERR	A/D	Focus error signal.
79	LDSLDERR	A/D	SLD error input of LD pick-up (when compatible is used).
80	FDMON	A/D	A/D input signal for disc judgment.

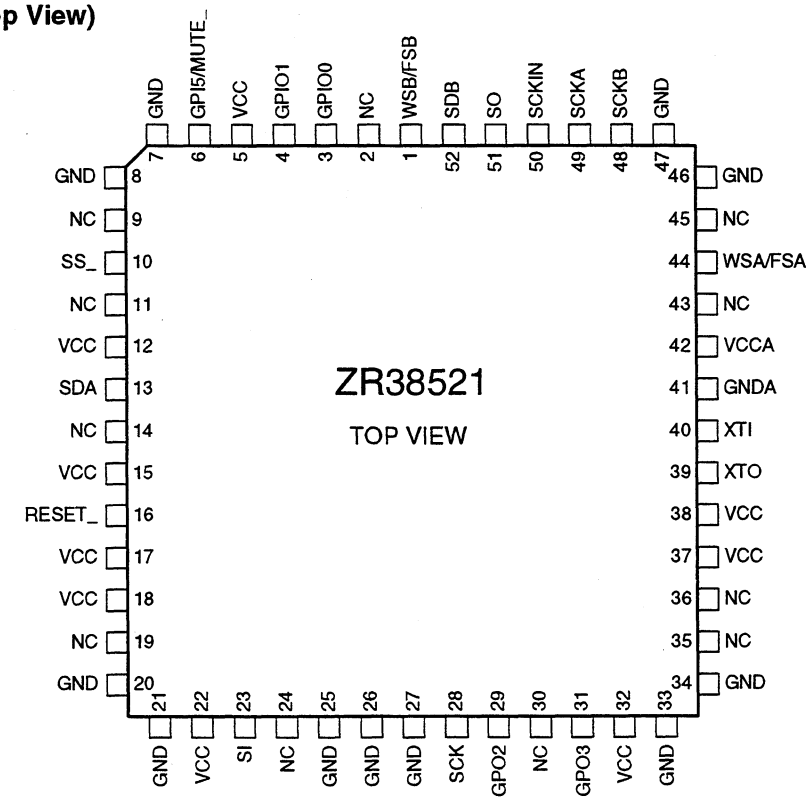
■ ZR38521 (DVD MAIN ASSY : IC301)

● AC-3 AUDIO DECODER

● Block Diagram



● Pin Assignment (Top View)



● Pin Function

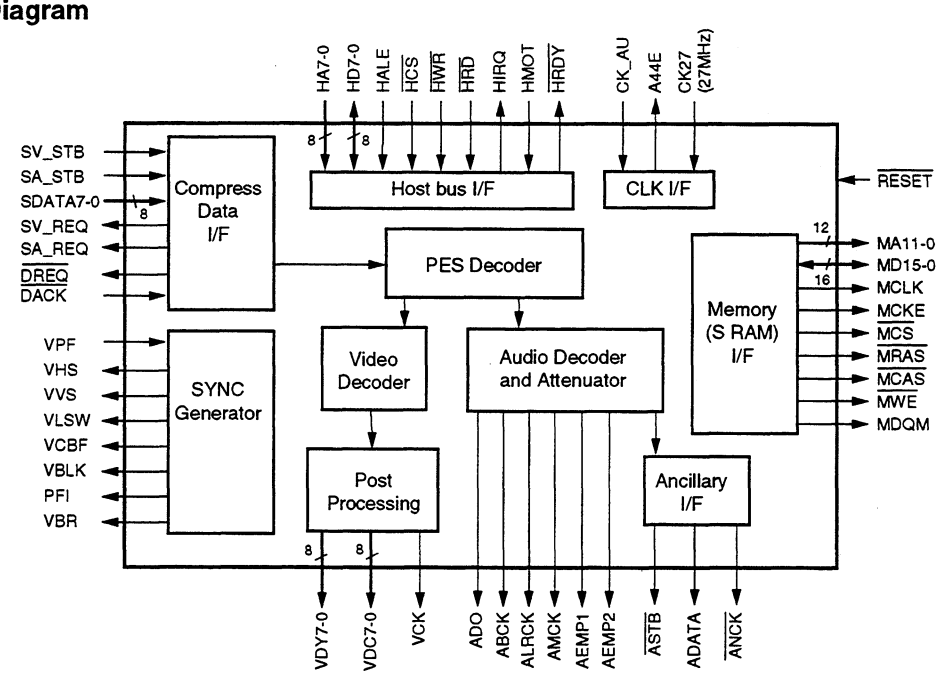
No.	Name	I/O	Function
1	WSB/FSB	I/O	Word selection or frame synchronous input/output for B Group serial port.
2	NC	-	Not used.
3	GPIO0	I/O	General-purpose I/O pin.
4	GPIO1	I/O	General-purpose I/O pin.
5	VCC	P	Power pin.
6	GPI5/MUTE	I	General-purpose input/mute pin.
7	GND	P	GND pin.
8	GND	P	GND pin.
9	NC	-	Not used.
10	SS_	I	Serial port interface: slave selection input (SPI).
11	NC	-	Not used.
12	VCC	P	Power pin.
13	SDA	I	Data input for serial port A.
14	NC	-	Not used.
15	VCC	P	Power pin.
16	RESET_	I	Reset input.
17	VCC	P	Power pin.
18	VCC	P	Power pin.
19	NC	-	Not used.
20	GND	P	GND pin.
21	GND	P	GND pin.
22	VCC	P	Power pin.
23	SI	I	Serial port interface: serial data input (SPI).
24	NC	-	Not used.
25	GND	I	GND pin.
26	GND	I	GND pin.
27	GND	P	GND pin.
28	SCK	I	Serial port interface: clock input (SPI).
29	GPO2	O	General-purpose output pin.
30	NC	-	Not used.
31	GPO3	O	General-purpose output pin.
32	VCC	P	Power pin.
33	GND	P	GND pin.
34	GND	P	GND pin.
35	NC	-	Not used.
36	NC	-	Not used.
37	VCC	P	Power pin.
38	VCC	P	Power pin.
39	XTO	O	Crystal oscillator output terminal.
40	XTI	I	Crystal oscillator input terminal.
41	GNDA	P	GND pin.
42	VCCA	P	Power pin.
43	NC	-	Not used.
44	WSA/FSA	I/O	Word selection or frame synchronous input/output for A Group serial port (for input).
45	NC	-	Not used.
46	GND	P	GND pin.
47	GND	P	GND pin.
48	SCKB	I/O	Clock input/output for B Group serial port.
49	SCKA	I/O	Clock input/output for A Group serial port.
50	SCKIN	I/O	Clock input/output for B Group serial port.
51	SO	O	Serial port interface: serial data output (SPI).
52	SDB	O	Data input for serial port B.

Note:
1) Connect an input terminal not to be used (TYPE = I) to VCC if active Low, or to GND if active High.
2) Do not connect output not to be used (TYPE = O), try state (TYPE = T), and NC terminal.

■ UPD61021 (DVD MAIN ASSY : IC401)

● MPEG2 DECODER

● Block Diagram



● Pin Function

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
1	MD7	I/O	Data bus for 16 bit memory interface	21	GND	–	Ground pin
2	MD6			22	MD9	I/O	Data bus for 16 bit memory interface
3	GND	–	Ground pin	23	MD8		
4	MD5	I/O	Data bus for 16 bit memory interface	24	VDD	–	Power supply pin
5	MD4			25	MDQM	O	Mask enable output signal of data input / output
6	VDD	–	Power supply pin	26	MCLK	O	81MHz system clock output for memory
7	MD3	I/O	Data bus for 16 bit memory interface	27	MCKE	O	Clock enable output signal
8	MD2			28	GND	–	Ground pin
9	GND	–	Ground pin	29	CK27	I	27MHz master clock input
10	MD1	I/O	Data bus for 16 bit memory interface	30	TCK81	I	Test clock pin Input 81MHz. Connect to GND in the actual use.
11	MD0			31	VDD	–	Power supply pin
12	VDD	–	Power supply pin	32	T_RESET	I	Test reset pin Connect to GND in the actual use.
13	MD15	I/O	Data bus for 16 bit memory interface	33	GND	–	Ground pin
14	MD14			34	T_PLL	I	PLL test input pin Connect to GND in the normal use.
15	GND	–	Ground pin	35	TPH0	O	Test output pin Open in the actual use.
16	MD13	I/O	Data bus for 16 bit memory interface	36	YPH1		
17	MD12			37	VDD	–	Power supply pin
18	VDD	–	Power supply pin	38	VPF	I	Freeze signal Input when freezing the picture. Freeze is able to performed by the software command.
19	MD11	I/O	Data bus for 16 bit memory interface	39	VFI	O	Field index signal output Discriminate the output picture data is ODD or EVEN.
20	MD10			40	VBR	O	Flag signal of the Video chroma Cb

No.	Pin Name	I/O	Pin Function
41	VBLK	O	Composite blanking output and clock reference signal Selectable by mode setting
42	VCBF	O	Color burst insertion position signal
43	VLSW	O	Line switch (at PAL used)
44	VVS	O	Vertical sync. signal output Also selectable to vertical reset signal by mode setting.
45	VHS	O	Horizontal sync. signal output Selectable to composite sync. signal or horizontal reset signal by mode register setting
46	GND	–	Ground pin
47	VCK	O	Video data clock output Frequency outputs to 27MHz and 13.5MHz.
48	VDD	–	Power supply pin
49	VDC0	O	Video chroma Cb and Cr output These pins output Cb and Cr video signal at 16 bit mode.
50	VDC1		
51	VDC2		
52	VDC3		
53	GND	–	Ground pin
54	VDC4	O	Video chroma Cb and Cr output These pins output Cb and Cr video signal at 16 bit mode.
55	VDC5		
56	VDC6		
57	VDC7		
58	VDD	–	Power supply pin
59	VDY0	O	Video data output Output Y data only at 16 bit mode. Output Cb, Y, Cr and Y video format at 8 bit mode.
60	VDY1		
61	VDY2		
62	VDY3		
63	GND	–	Ground pin
64	VDY4	O	Video data output Output Y data only at 16 bit mode. Output Cb, Y, Cr and Y video format at 8 bit mode.
65	VDY5		
66	VDY6		
67	VDY7		
68	VDD	–	Power supply pin
69	ADO	O	PCM data output
70	ABCK	O	Audio data clock output
71	ALRCK	O	LR switching signal
72	AMCK	O	Master clock for audio Outputs same frequency as CK_AU pin
73	AEMP2	O	Emphasis output When existing the emphasis in conformity to 50 / 15μs, outputs "H".
74	AEMP1	O	Emphasis output When existing the emphasis in conformity to ITU-TJ.71, outputs "H".
75	$\overline{\text{ASTB}}$	O	Ancillary strobe signal
76	ADATA	O	Ancillary data output

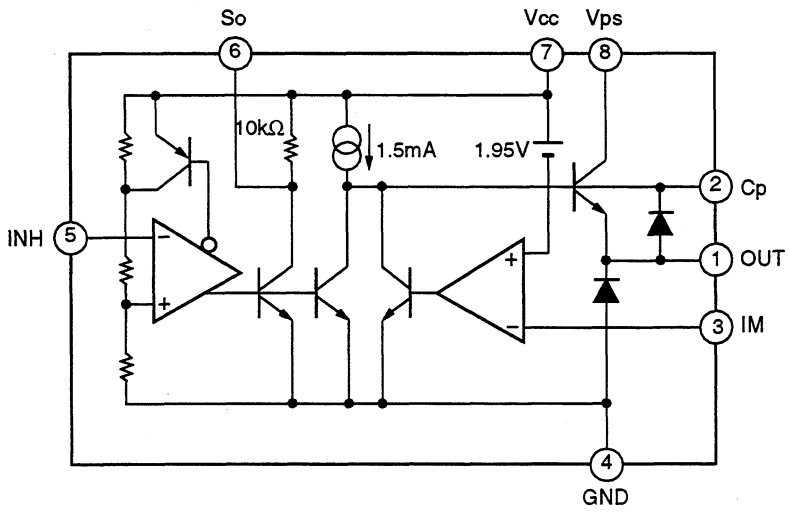
No.	Pin Name	I/O	Pin Function
77	$\overline{\text{ANCK}}$	O	Clock signal at ancillary data output
78	GND	–	Ground pin
79	$\overline{\text{DREQ}}$	O	Request signal when stream input via the host path.
80	$\overline{\text{DACK}}$	I	Acknowledge signal when stream input via the host path.
81	A44E	O	Status signal of sampling clock of the decode When compound with 44.1kHz, it becomes "H".
82	CK_AU	I	Audio sampling clock input
83	VDD	–	Power supply pin
84	$\overline{\text{RESET}}$	I	Reset input
85	HMOT	I	Host interface mode selection HMOT : When set to H, it becomes bus mode of 68 system.
86	HIRQ	O	Interrupt request signal to the host This pin becomes active when accepting the interrupt. This pin is tri-state output.
87	$\overline{\text{HRDY}}$	O	Tri-state ready output Communicate the end of bus cycle to the host CPU in the 68k mode. Use for Wait signal in the 78k0 mode.
88	$\overline{\text{HWR}}$	I	Enable signal when the host is wrote Input WR signal in the 78k bus mode. Input R/W signal in the 68k bus mode.
89	$\overline{\text{HRD}}$	I	Enable signal when the host is readed Input RD signal in the 78k bus mode. Input data strobe signal in the 68k bus mode.
90	$\overline{\text{HCS}}$	I	Chip select signal of active "L"
91	HALE	I	Address latch enable signal When address and data is not multiplexed, pull-up to "H".
92	GND	–	Ground pin
93	HD0	I/O	Data bus for 8 bit host interface Lower 8 bit address of the host is able to input with multiplex.
94	HD1		
95	HD2		
96	HD3		
97	VDD	–	Power supply pin
98	HD4	I/O	Data bus for 8 bit host interface Lower 8 bit address of the host is able to input with multiplex.
99	HD5		
100	HD6		
101	HD7		
102	GND	–	Ground pin
103	HA0	I	Host address bus input This address bus is able to multipled to HD7-0
104	HA1		
105	HA2		
106	HA3		
107	VDD	–	Power supply pin
108	HA4	I	Host address bus input This address bus is able to multipled to HD7-0
109	HA5		
110	HA6		
111	HA7		
112	GND	–	Ground pin

No.	Pin Name	I/O	Pin Function	No.	Pin Name	I/O	Pin Function
113	TM0	I	Test mode input Connect to GND excepting test.	137	MST4	O	Test output Set to open in the actual use.
114	TM1			138	MST3		
115	TS0	O	Test output Set to open in the actual use.	139	MST2		
116	TS1			140	MST1		
117	TS2			141	MST0		
118	TS3			142	VDD	–	Power supply pin
119	TS4			143	MA9	O	Address output Output low address to MA11-0 and column address to MA8-0 with multiplex.
120	TS5			144	MA8		
121	VDD	–	Power supply pin	145	MA7		
122	SDATA7	I	A/V PES stream data bus	146	MA6		
123	SDATA6			147	MA5		
124	SDATA5			148	MA4		
125	SDATA4			149	GND	–	Ground pin
126	GND	–	Ground pin	150	MA3	O	Address output Output low address to MA11-0 and column address to MA8-0 with multiplex.
127	SDATA3	I	A/V PES stream data bus	151	MA2		
128	SDATA2			152	MA1		
129	SDATA1			153	MA0		
130	SDATA0			154	MA10		
131	VDD	–	Power supply pin	155	MA11		
132	SV_STB	I	Video PES stream data strobe signal	156	MCS	O	Chip select output
133	$\overline{\text{SA\_STB}}$	I	Audio PES stream data strobe signal	157	$\overline{\text{MRAS}}$	O	Low address strobe signal
134	$\overline{\text{SV\_REQ}}$	O	Video PES stream data request signal	158	$\overline{\text{MCAS}}$	O	Column address strobe signal
135	$\overline{\text{SA\_REQ}}$	O	Audio PES stream data request signal	159	$\overline{\text{MWE}}$	O	Write enable signal
136	$\overline{\text{GND}}$	–	Ground pin	160	$\overline{\text{VDD}}$	–	Power supply pin

■ IR3C07N (DVD MAIN ASSY : IC995)

● LASER DIODE DRIVER

● Block Diagram



● Pin Function

No.	Mark	Pin Function
1	OUT	Output
2	Cp	Phase compensation
3	IM	Monitor input
4	GND	Ground
5	INH	Inhibit input (ON, OFF)
6	So	Operating signal output
7	Vcc	Power supply for control circuit
8	Vps	Power supply for laser driver

■ UPD4516161G5-A12-7JF (DVD MAIN ASSY : IC421)

● SYNCHRONOUS DRAM

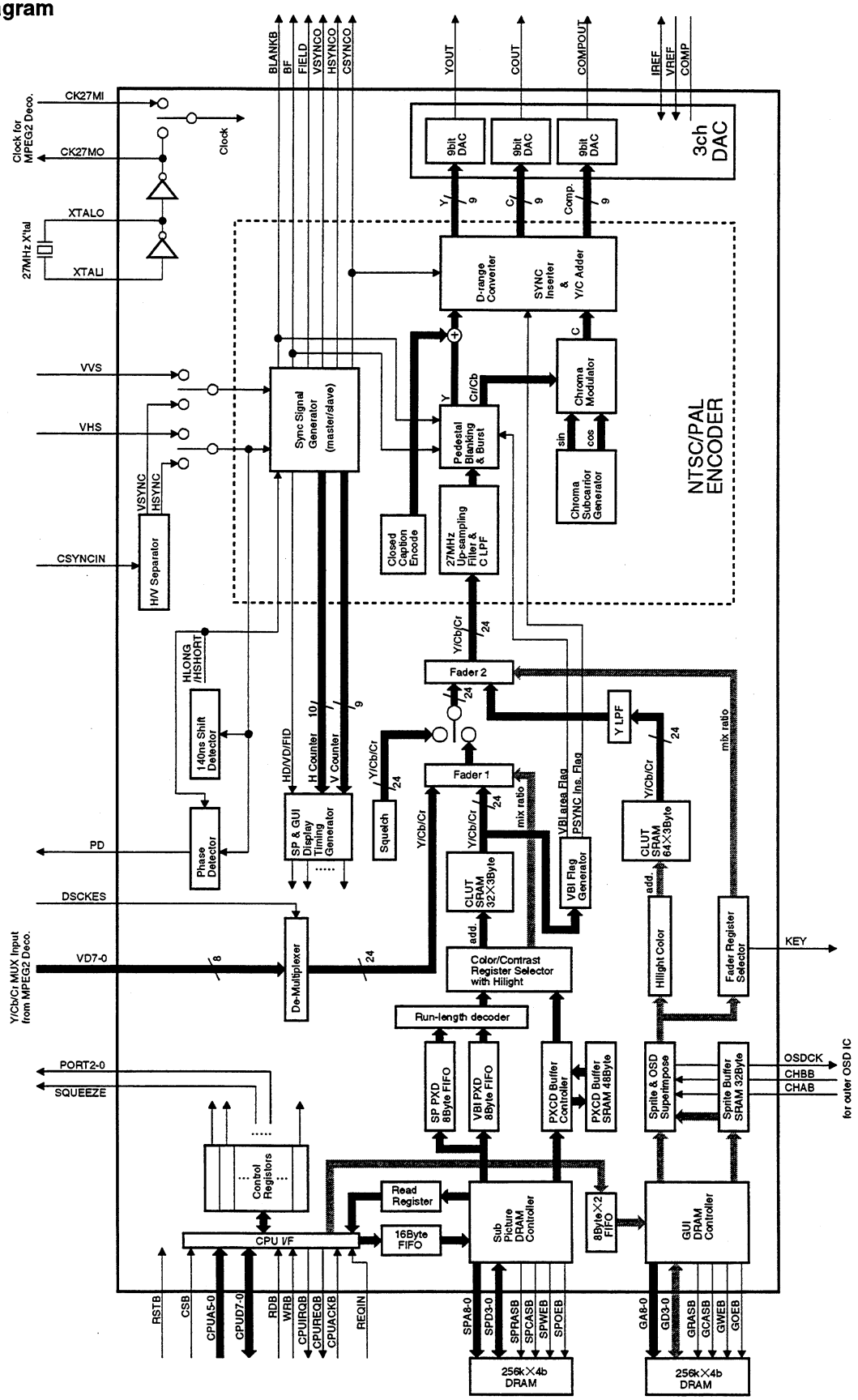
● Pin Function

No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	Vcc	Power supply	26	Vss	Ground
2	DQ0	Data input/output	27	A4	Address input
3	DQ1		28	A5	
4	VssQ	Ground for DQ	29	A6	
5	DQ2	Data input/output	30	A7	
6	DQ3		31	A8	
7	VccQ	Power supply for DQ	32	A9	
8	DQ4	Data input/output	33	NC	Non connection
9	DQ5		34	CKE	Clock enable
10	VssQ	Ground for DQ	35	CLK	System clock input
11	DQ6	Data input/output	36	UDQM	Upper DQ mask enable
12	DQ7		37	NC	Non connection
13	VccQ	Power supply for DQ	38	VccQ	Power supply for DQ
14	LDQM	Low DQ mask enable	39	DQ8	Data input/output
15	$\overline{WE}$	Write enable	40	DQ9	
16	$\overline{CAS}$	Column address strobe	41	VssQ	Ground for DQ
17	$\overline{RAS}$	Row address strobe	42	DQ10	Data input/output
18	$\overline{CS}$	Chip select	43	DQ11	
19	A11	Address input	44	VccQ	Power supply for DQ
20	A10		45	DQ12	Data input/output
21	A0		46	DQ13	
22	A1		47	VssQ	Ground for DQ
23	A2		48	DQ14	Data input/output
24	A3		49	DQ15	
25	Vcc	Power supply	50	Vss	Ground

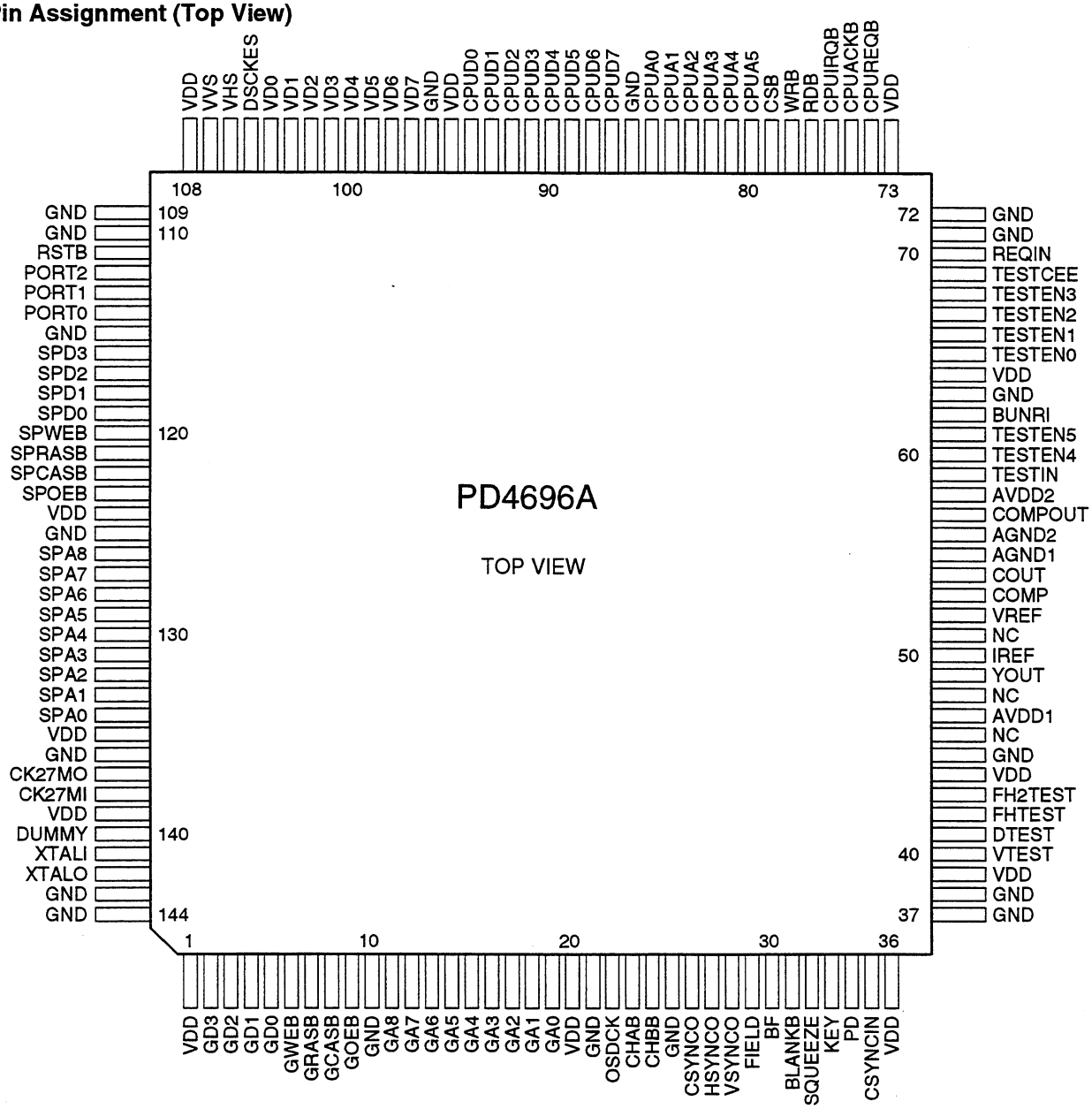
■ PD4696A (DVD MAIN ASSY : IC501)

● VIDEO ENCODER

● Block Diagram



● Pin Assignment (Top View)



● Pin Function

No.	Name	I/O	Function
1	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
2	GD3	I/O	DRAM data input/output for GUI. Connect to data input/output of 256 k54 bits DRAM.
3	GD2		
4	GD1		
5	GD0		
6	GWEB	O	/WE output to DRAM for GUI. Connect to the /WE terminal of 256 k54 bits DRAM.
7	GRASB	O	/RAS output to DRAM for GUI. Connect to the /RAS terminal of 256 k54 bits DRAM.
8	GCASB	O	/CAS output to DRAM for GUI. Connect to the /CAS terminal of 256 k54 bits DRAM.
9	GOEB	O	/OE output to DRAM for GUI. Connect to the /OE terminal of 256 k54 bits DRAM.
10	GND	-	Grounding terminal. Connect to GND (GND of the logic system).

No.	Name	I/O	Function
11	GA8	O	Address output of DRAM for GUI. Connect to address output of 256 k54 bits DRAM. GAO is LSB, and GA8 is MSB.
12	GA7		
13	GA6		
14	GA5		
15	GA4		
16	GA3		
17	GA2		
18	GA1		
19	GA0		
20	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
21	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
22	OSDCK	O	Clock output when using OSD IC as external. Connect to clock input of OSD IC (6.75 MHz).
23	CHAB	I	Connects character output of OSD IC when using the OSD IC as external. Character colors fom the color pallet according to OSD mode will be superimposed on video output when the system is set to "L".
24	CHBB	I	Connects character frame output of OSD IC when using the OSD IC as external. Character frame colors from the color pallet according to OSD mode will be superimposed on video output when the system is set to "L".
25	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
26	CSYNCO	O	Composite sync output from built-in SSG. Synchronizes video output (negative logic).
27	HSYNCO	O	H sync output from built-in SSG. Synchronizes video output (negative logic).
28	VSYNCO	O	V sync output from built-in SSG. Synchronizes video output (negative logic).
29	FIELD	O	Field output from built-in SSG. Synchronizes the field of video output. Indicates "Odd" when the system is set to "H" and "Even" when "L".
30	BF	O	Burst flag output from built-in SSG. The system indicates the position of burst of video output with "H".
31	BLANKB	O	Blanking output from built-in SSG. The system indicates the blanking area between H and V of video output with "L".
32	SQUEEZE	O	Outputs the content of built-in register of the same name.
33	KEY	O	Outputs "H" if the value of fader corresponding the value of pixel of GUI is other than zero (0) when the value of KEY_EN register is "H" Otherwise outputs "L" Synchronizes the pixel position of video output (delay is also possible). The system is fixed.
34	PD	O	Outputs the result of comparison of phases of H sync of external input and H sync of built-in SSG in three states. "L"/"H" shows the polarity, and the pulse width shows the phase difference. ON/OFF and polarity of output are set by the register.
35	CSYNCIN	I	Composite sync input for external synchronization. The composite sync separates into H sync and V sync inside the system to synchronize built-in SSG or output the results of comparison of H phases from PD.
36	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
37	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
38	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
39	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
40	VTEST	-	Test terminal. Leave it open (terminal for IC test).
41	DTEST		
42	FHTEST		
43	FH2TEST		
44	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
45	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
46	NC	-	No connection. Leave it open.
47	AVDD1	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
48	NC	-	No connection. Leave it open.
49	YOUT	O	Analog video output of luminance signal. Composite sync signal is superimposed. Connect the load of standard 150Ωbetween GND of the analog system.
50	IREF	I	Terminal for adjustment of video output current (full-scale current). Connect the reference resistor of standard 1.1kΩ between GND of the analog system.
51	NC	-	No connection. Leave it open.
52	VREF	I	Terminal for adjustment of video output current (full-scale current). Apply the reference voltage of standard 1.0V.
53	COMP	I	Terminal to compensate phase of built-in DA convertor. Connect the capacitor of standard 0.1ΩF between GND of the analog system.
54	COUT	O	Analog video output of color signal. Connect the load of standard 150Ω between GND of the analog system.
55	AGND1	-	Grounding terminal. Connect to GND (GND of the analog system).
56	AGND2	-	Grounding terminal. Connect to GND (GND of the analog system).
57	COMPOUT	O	Analog video output of composite video signal. Composite sync signal is superimposed. Connect the load of standard 150â+ between GND of the analog system.
58	AVDD2	-	Power terminal. Connect to +3.3 V (VDD of the analog system).
59	TESTIN	-	Test terminal. Leave it open (terminal for IC test).
60	TESTEN4		
61	TESTEN5		
62	BUNRI		

PD4696A

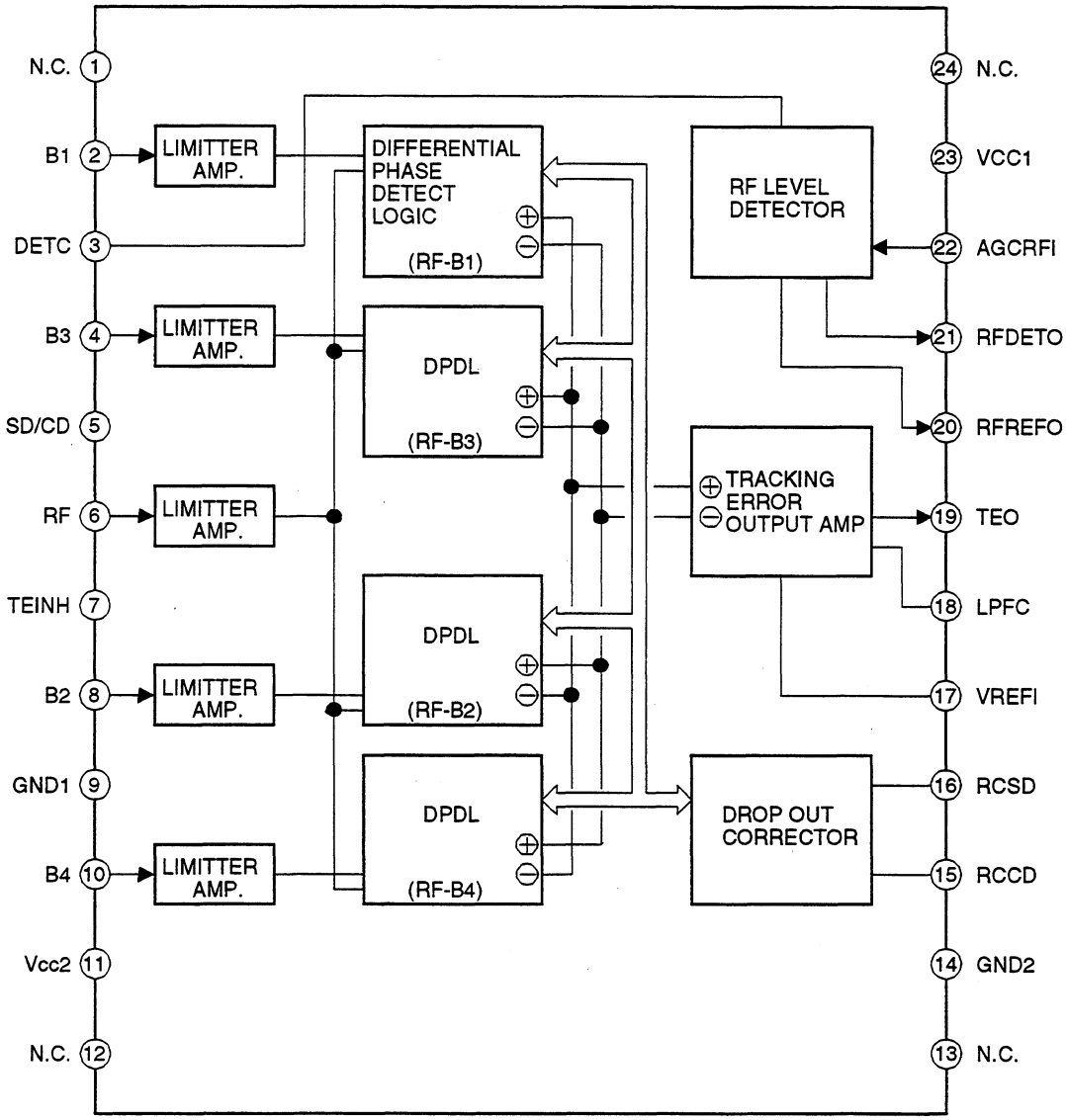
No.	Name	I/O	Function
63	GND	-	Grounding terminal. Connect to GND (GND of the analog system).
64	VDD	-	Power terminal. Connect to +3.3 V (VDD of the analog system).
65	TESTEN0	-	Test terminal. Leave it open (terminal for IC test)
66	TESTEN1		
67	TESTEN2		
68	TESTEN3		
69	TESTCCE		
70	REQIN	I	Inputs request signal of the DMA source if OR logic is required for transfer enable request of the external IC (DMA source) and DMA request of this IC.
71	GND	-	Grounding terminal. Connect to GND (GND of the analog system).
72	GND	-	Grounding terminal. Connect to GND (GND of the analog system).
73	VDD	-	Power terminal. Connect to +3.3 V (VDD of the analog system).
74	CPUREQB	O	DMA request signal. Connect to DMA request input of CPU IC. The DMA request is roughly classified into the request for subvideo data and the request for GUI data. Either requests are executed by the instruction of the DMA start command to the corresponding register. The "L" level of the DMA request signal indicates that the request is being made. The system automatically sets to "H" if built-in FIFO becomes full or transmission of the required amount of data is completed. THe DMA request signal can use OR logic with REQIN input.
75	CPUACKB	I	Connect acknowledge output from CPU IC during DMA request. The system retrieves data input to CPUD7-0 into biult-in FIFO at the leading edge of this signal.
76	CPUIRQB	O	Interrupt signal to CPU IC. Connect to interrupt input of CPU IC. The system generates "L" signal every time the V blanking of video output is encountered.
77	RDB	I	Read signal when the CPU IC wants to read the content of the read register. The content of the register of the address being accessed will be output to CPU7-0 when the system is set to "L".
78	WRB	I	Write signal when the CPU IC wants to rewrite the content of the read register. Connects write output of CPU IC. The content of the register of the address being accessed will be rewritten to the data being input to CPU7-0 when the system is set to "L".
79	CSB	I	Selection signal when the CPU IC wants to read or write the register of this IC. Connects CS output of CPU IC.
80	CPUA5	I	Address signal when the CPU IC wants to read or write the register of this IC. Connects address output of CPU IC. CPUA0 is LSB, and CPUA5 is MSB.
81	CPUA4		
82	CPUA3		
83	CPUA2		
84	CPUAI		
85	CPUAO		
86	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
87	CPUD7	IO	Data signal when the CPU IC wants to read or write the register of this IC, and transmission data signal during DMA transmission. Connects to data bus under the CPU IC. CPUD0 is LSB, and CPUD7 is MSB.
88	CPUD6		
89	CPUD5		
90	CPUD4		
91	CPUD3		
92	CPUD2		
93	CPUD1		
94	CPUD0		
95	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
96	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
97	VD7	I	Connects video data signal output of 8-bit multiplex mode of the MPEG2 decoder IC. VD0 is LSB, and VD7 is MSB.
98	VD6		
99	VD5		
100	VD4		
101	VD3		
102	VD2		
103	VD1		
104	VD0		
105	DSCKES	I	Signal to select whether retrieve video data signal input from VD7-0 at the leading edge or trailing edge of the internal 27 MHz clock. The system selects the leading edge at "L" or open, and selects the trailing edge at "H".
106	VHS	I	Connects H sync output from the MPEG2 decoder. Must be synchronized with VD7-0 (negative logic). Synchronizes built-in SSG, and outputs the result of comparison of H phases from PD.
107	VVS	I	Connects V sync output from the MPEG2 decoder. Must be synchronized with VD7-0 (negative logic). Synchronizes built-in SSG.
108	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
109	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
110	GND	-	Grounding terminal. Connect to GND (GND of the logic system).

No.	Name	I/O	Function
111	RSTB	I	Reset input for IC as a whole. The built-in register, circuitry, etc. will be initialized when the system is set to "L".
112	PORT2	O	Outputs the content of the built-in register of the same name.
113	PORT1		
114	PORT0		
115	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
116	SPD3	IO	Data input/output of DRAM for subvideo. Connect to data input/output of 256 kü~4 bits DRAM.
117	SPD2		
118	SPD1		
119	SPD0		
120	SPWEB	O	/WE output to DRAM for subvideo. Connect to the /WE terminal of 256 k54 bits DRAM.
121	SPRASB	O	/RAS output to DRAM for subvideo. Connect to the /RAS terminal of 256 k54 bits DRAM.
122	SPCASB	O	/CAS output to DRAM for subvideo. Connect to the /CAS terminal of 256 k54 bits DRAM.
123	SPOEB	O	/OE output to DRAM for subvideo. Connect to the /OE terminal of 256 k54 bits DRAM.
124	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
125	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
126	SPA8	O	Address output of DRAM for subvideo. Connect to address output of 256 k54 bits DRAM. SPA0 is LSB, and SPA8 is MSB.
127	SPA7		
128	SPA6		
129	SPA5		
130	SPA4		
131	SPA3		
132	SPA2		
133	SPA1		
134	SPA0		
135	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
136	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
137	CK27M0	O	27 MHz clock output from built-in X'tal OSC. The terminal is buffered, and can drive external circuit.
138	CK27MI	I	27 MHz system clock input during external input mode of this IC. Inputs rectangular wave of 27 MHz.
139	VDD	-	Power terminal. Connect to +3.3 V (VDD of the logic system).
140	DUMMY	O	Dummy output of built-in X'tal OSC. Normally leave it open.
141	XTALI	I	Input of built-in X'tal OSC. Use the terminal by connecting the X'tal to external circuit.
142	XTALO	O	Output of built-in X'tal OSC. Use the terminal by connecting the X'tal to external. Cannot supply the clock to external circuit from this terminal. Should use CK27MO. For the system clock of this IC, this signal is internally buffered during internal input.
143	GND	-	Grounding terminal. Connect to GND (GND of the logic system).
144	GND	-	Grounding terminal. Connect to GND (GND of the logic system).

■ PA0065AM (DVD MAIN ASSY : IC601)

● TIME-DIFFERENCE IC

● Block Diagram



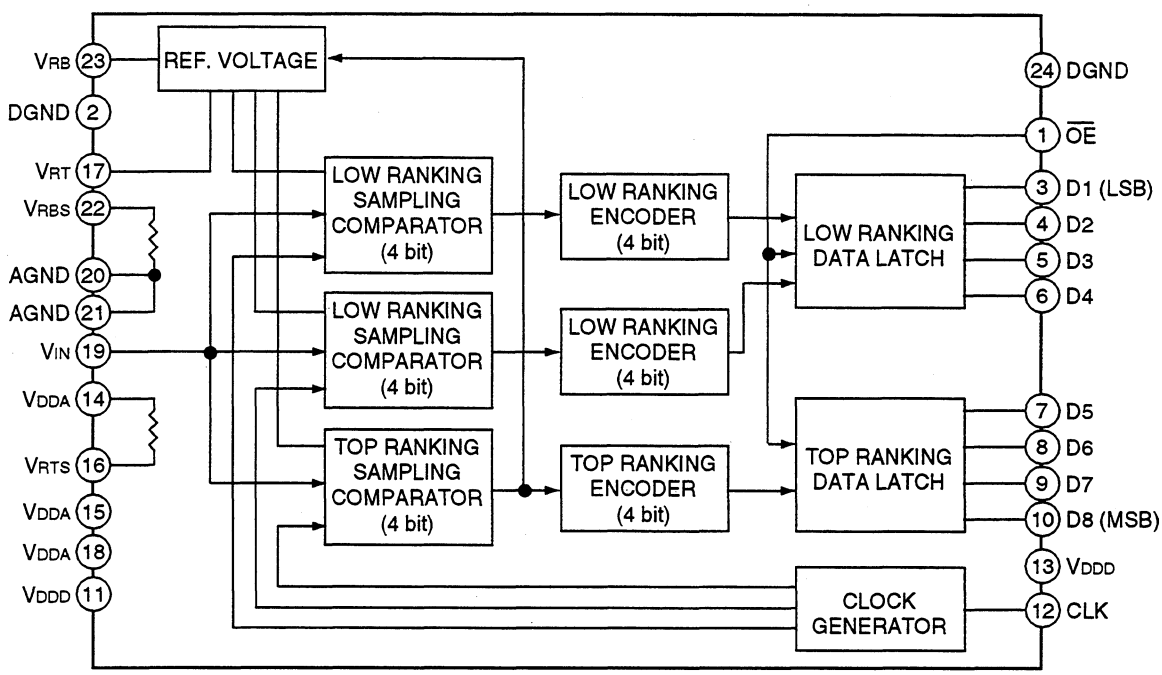
● Pin Function

No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	NC	Non connection	13	NC	Non connection
2	B1	B1 signal input	14	GND2	Ground
3	DETC	Connect a capacitor for RF level detection	15	RCCD	Time constant for limit the pulse width of CD mode
4	B3	B3 signal input	16	RCDVD	Time constant for limit the pulse width of DVD mode
5	DVD/CD	DVD/CD mode switching signal input H : DVD mode, L : CD mode	17	VREFI	Reference voltage input
6	RF	RF signal input	18	LPFC	Low pass filter for TE output
7	TEINH	TE output prohibition signal input	19	TEO	TE output
8	B2	B2 signal input	20	RFREFO	Reference voltage output for RF level detection
9	GND1	Ground	21	RFDETO	RF level detecting output
10	B4	B4 signal input	22	AGCRFI	AGCRF signal input
11	VCC2	5V power supply	23	VCC1	5V power supply
12	NC	Non connection	24	NC	Non connection

■ TLC5540INS (DVD MAIN ASSY : IC731)

● A/D CONVERTER

● Block Diagram



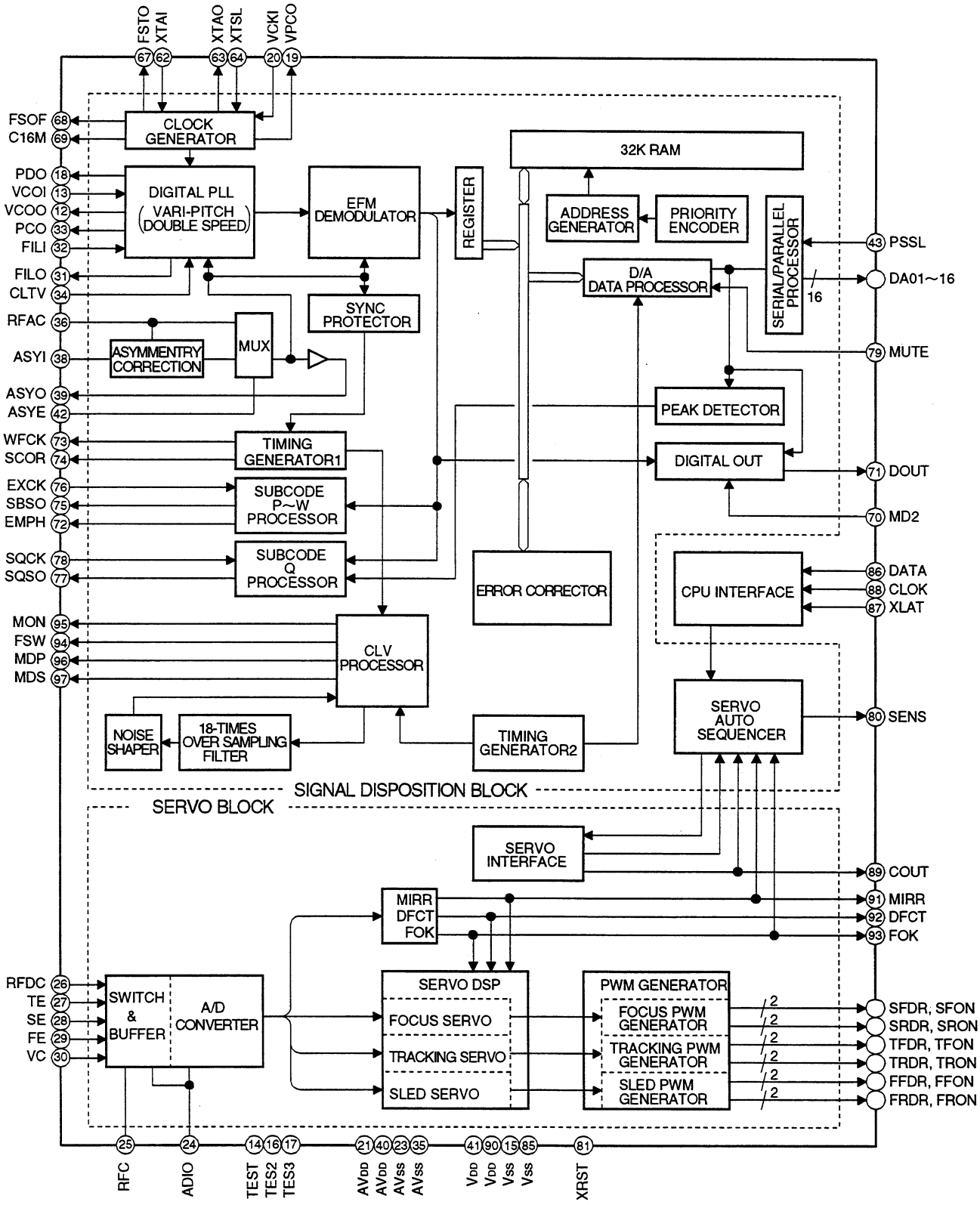
● Pin Function

No.	Pin Name	I/O	Pin Function
1	$\overline{OE}$	I	Output enable $\overline{OE}$="L" level : Data enable $\overline{OE}$="H" level : Output high impedance
2, 24	DGND	—	Ground for Digital system
3-10	D1-D8	O	Digital output D1: LSB, D8 : MSB
11, 13	VDDD	—	Power supply for Digital system
12	CLK	I	Clock input
16	VRTS	—	Reference voltage output (upper) Short-circuit to VRT in the internal reference voltage used. Generates a 2.63V.
17	VRT	I	Reference voltage output (upper)
23	VRB	I	Reference voltage output (lower)
14, 15, 18	VDDA	—	Power supply for Analog system
19	VIN	I	Analog input
20, 21	AGND	—	Ground for Analog system
22	VRBS	—	Reference voltage output (upper) Short-circuit to VRT in the internal reference voltage used. Generates a 0.61V.

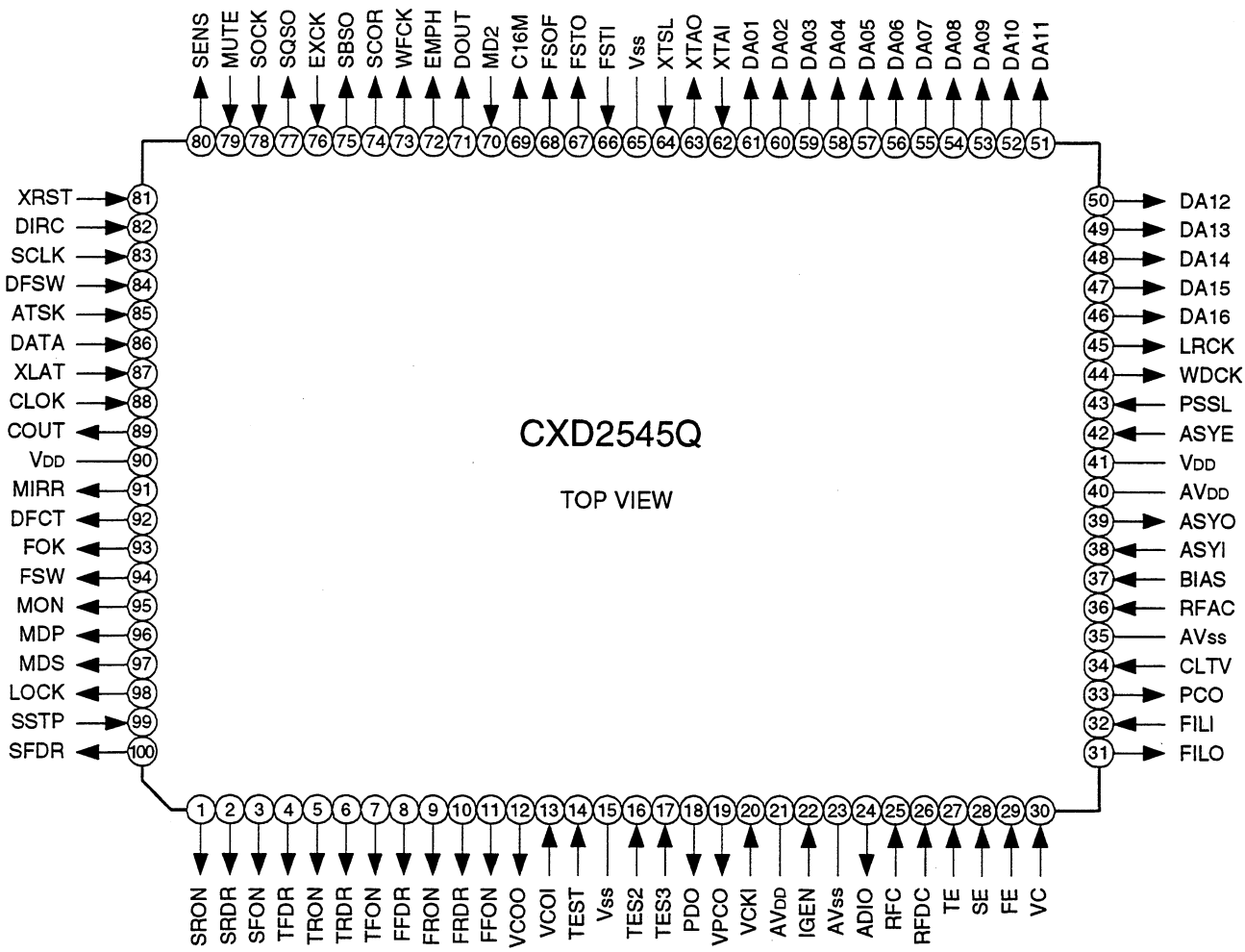
■ CXD2545Q (DVD MAIN ASSY : IC801)

● DIGITAL SERVO IC

● Block Diagram



● Pin Assignment (Top View)



● Pin Function

No.	Name	I/O	Function
1	SRON	O	Thread drive output.
2	SRDR	O	
3	SFON	O	
4	TFDR	O	Tracking drive output.
5	TRON	O	
6	TRDR	O	
7	TFON	O	
8	FFDR	O	Focus drive output.
9	FRON	O	
10	FRDR	O	
11	FFON	O	
12	VCOO	O	Oscillation circuit output for analog EFM PLL.
13	VCOI	I	Oscillation circuit input for analog EFM PLL. fLOCK = 8.6436MHz.
14	TEST	I	TEST terminal. Normally GND.
15	Vss	-	Digital GND.
16	TES2	I	TEST terminal. Normally GND.
17	TES3	I	TEST terminal. Normally GND.
18	PDO	O	Charge-pump output for analog EFM PLL.
19	VPCO	O	PLL charge-pump output for variable pitch.
20	VCKI	I	Clock input from external VCO for variable pitch.fcenter = 16.9344MHz.

No.	Name	I/O	Function
21	AVDD	-	Analog power supply.
22	IGEN	I	Terminal to connect the current source reference resistor of the operational amplifier for digital servo.
23	AVss	-	Analog GND.
24	ADIO	O	A/D converter input monitor terminal.
25	RFC	I	Terminal to connect the low-pass filter capacitor for RFDC input.
26	RFDC	I	RF signal input. Input range: 2.15 to 5.0 V (when VDD = AVDD = 5.0 V).
27	TE	I	Tracking error signal input. Input range: 2.5~1.0 V (when VDD = AVDD = 5.0 V).
28	SE	I	Thread-error signal input. Input range: 2.5~1.0 V (when VDD = AVDD = 5.0 V).
29	FE	I	Focus-error signal input. Input range: 2.5~1.0 V (when VDD = AVDD = 5.0 V).
30	VC	I	Mid-point voltage input terminal.
31	FILO	O	Filter output for master PLL.
32	FILI	O	Filter input for master PLL.
33	PCO	O	Charge-pump output for master PLL.
34	CLTV	I	VCO control voltage input for master.
35	AVss	-	Analog GND.
36	RFAC	I	EFM signal input.
37	BIAS	I	Asymmetrical circuit constant current input.
38	ASYI	I	Asymmetrical comparison voltage input.
39	ASYO	O	EFM full-swing output (L = Vss, H = VDD).
40	AVDD	-	Analog power supply.
41	VDD	-	Digital power supply.
42	ASYE	I	Asymmetrical circuit ON/OFF (L = OFF, H = ON).
43	PSSL	I	Audio data output mode switching input (L = serial output, H = parallel output).
44	WDCK	O	48-bit slot D/A interface. Word clock (f = 2 Fs).
45	LRCK	O	48-bit slot D/A interface. OR clock (f = Fs).
46	DA16	O	DA16 output when PSSL = 1. Serial data of 48-bit slot when PSSL = 0.
47	DA15	O	DA15 output when PSSL = 1. Bit clock of 48-bit slot when PSSL = 0.
48	DA14	O	DA14 output when PSSL = 1. Serial data of 64-bit slot when PSSL = 0.
49	DA13	O	DA13 output when PSSL = 1. Bit clock of 64-bit slot when PSSL = 0.
50	DA12	O	DA12 output when PSSL = 1. LR clock of 64-bit slot when PSSL = 0.
51	DA11	O	DA11 output when PSSL = 1. GTOP output when PSSL = 0.
52	DA10	O	DA10 output when PSSL = 1. XUGF output when PSSL = 0.
53	DA09	O	DA09 output when PSSL = 1. XPLCK output when PSSL = 0.
54	DA08	O	DA08 output when PSSL = 1. GFS output when PSSL = 0.
55	DA07	O	DA07 output when PSSL = 1. RFCK output when PSSL = 0.
56	DA06	O	DA06 output when PSSL = 1. C2PO output when PSSL = 0.
57	DA05	O	DA05 output when PSSL = 1. XRAOF output when PSSL = 0.
58	DA04	O	DA04 output when PSSL = 1. MNT3 output when PSSL = 0.
59	DA03	O	DA03~ output when PSSL = 1. MNT2 output when PSSL = 0.
60	DA02	O	DA02 output when PSSL = 1. MNT1 output when PSSL = 0.
61	DA01	O	DA01 output when PSSL = 1. MNT0 output when PSSL = 0.
62	XTAI	1	X'tal oscillation circuit input. 16.9344 MHz or 33.8688 MHz input.
63	XTAO	O	X'tal oscillation circuit output.
64	XTSL	I	X'tal selective input terminal. The system is set to L when X+tal is 16,9344 MHz, and H when 33,8688 MHz (during normal playback).
65	Vss	-	Digital GND.
66	FSTI	I	Reference clock input terminal for digital servo block.
67	FSTO	O	2/3 divided output for Terminals 62 and 63. Variable pitch does not change the output.
68	FSOF	O	1/4 divided output for Terminals 62 and 63. Variable pitch does not change the output.
69	C16M	O	16,9344 MHz output. Changes simultaneously with variable pitch (during normal playback).
70	MD2	I	Digital-Out ON/OFF control terminal (L = OFF, H = ON).
71	DOUT	O	Digital-Out output terminal.
72	EMPH	O	Emphasis mode output of the disc played back (L = no emphasis, H = emphasis).
73	WFCK	O	WFCK output.
74	SCOR	O	Subcode sync output terminal (The system sets to H when either subcode sync S0 or S1 is detected.).
75	SBSO	O	Serial output of Sub-P to Sub W.

No.	Name	I/O	Function
76	EXCK	I	Clock input for SBSO read out.
77	SQSO	O	Sub-Q 80-bit output, PCM peak data, level data 16-bit output.
78	SQCK	I	Clock input for SBSO read out.
79	MUTE	I	Mute switching terminal (H = Mute).
80	SENS	O	SENS output. Outputs to CPU.
81	XRST	I	System reset (L = reset).
82	DIRC	I	Used when skipping a single track. (Inputs VDD level when not used.)
83	SCLK	I	Clock for reading SENS serial data.
84	DFSW	I	DFCT switching terminal (H = DFCT measure circuit OFF).
85	ATSK	I	Antishock terminal.
86	DATA	I	Inputs serial data from the CPU.
87	XLAT	I	Inputs latch from the CPU.
88	CLOK	I	Inputs serial data transfer clock from the CPU.
89	COUT	O	Track counting signal output.
90	VDD	-	Digital power supply.
91	MIRR	O	Mirror signal output.
92	DFCT	O	Defect signal output.
93	FOK	O	Focus OK output.
94	FSW	O	Outputs switching the output filter of the spindle motor.
95	MON	O	ON/OFF control output for the spindle motor.
96	MDP	O	Servo control of the spindle motor.
97	MDS	O	Servo control of the spindle motor.
98	LOCK	O	Samples GFS at 460 Hz and outputs H when GFS is H. Outputs L if GFS is L eight times continuously.
99	SSTP	I	Terminal for the signal to detect the most inner circumference of the disc.
100	SFDR	O	Thread drive output.

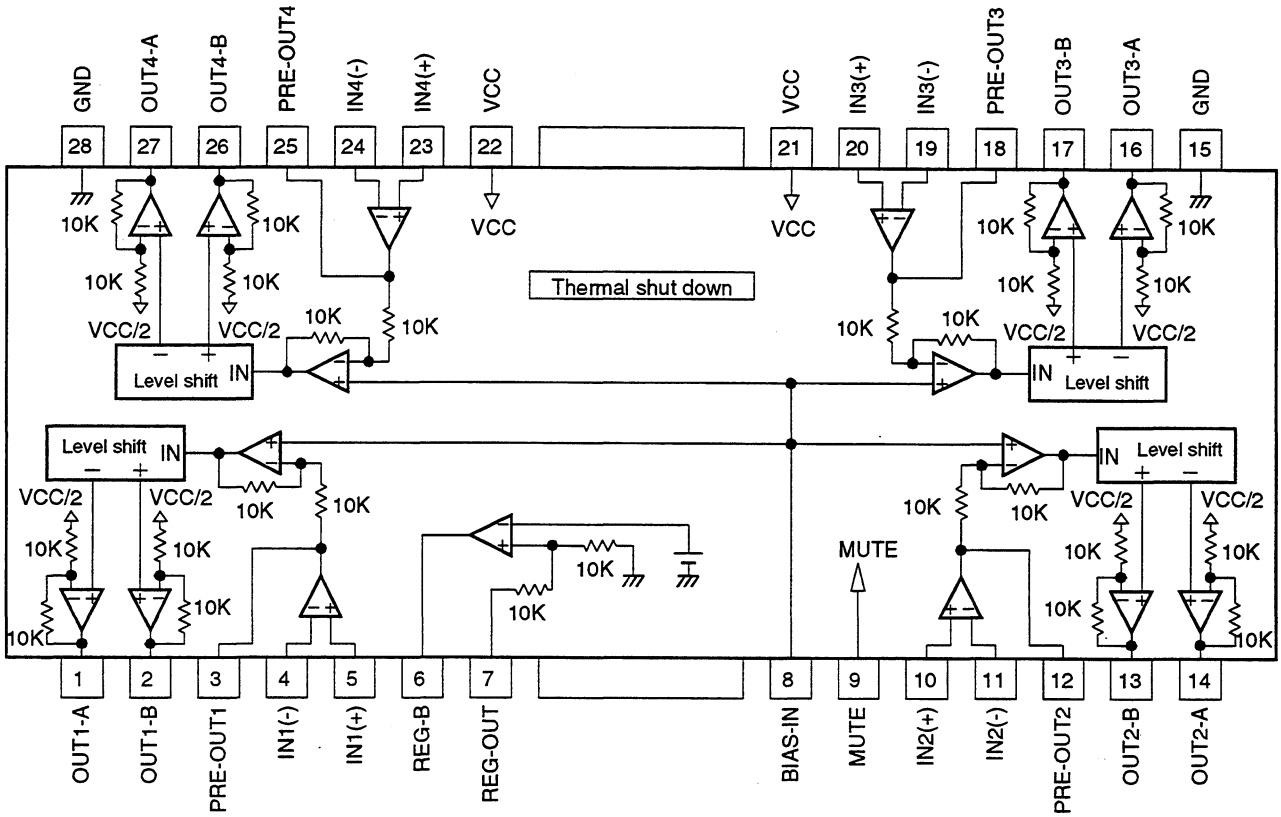
Notes:

- The 64-bit slot is 2's complementary output of LSB first. The 48-bit slot is 2's complementary output of MSB first.
- GTOP is to monitor protection of Frame sync (H: sync protective window open).
- XUGF is Frame sync obtained from EFM signal, and is negative pulse. It is signal before sync protection. "
- For XPLCK, PLL is produced so that the reverse and trailing edge of the clock of EFM PLL meet the point of change of EFM signal.
- GFS signal is set to H when Frame sync meets the interpolated protection timing.
- RFCK is obtained with X'tal precision. It is signal of cycles at 136±s.
- C2PO is signal to express error status of data.
- XRAOF is signal generated when 32K RAM exceeds the jitter margin ofü}28 frames.

■ BA6797FP (DVD MAIN ASSY : IC851)

● BTL DRIVER

● Block Diagram



● Pin Function

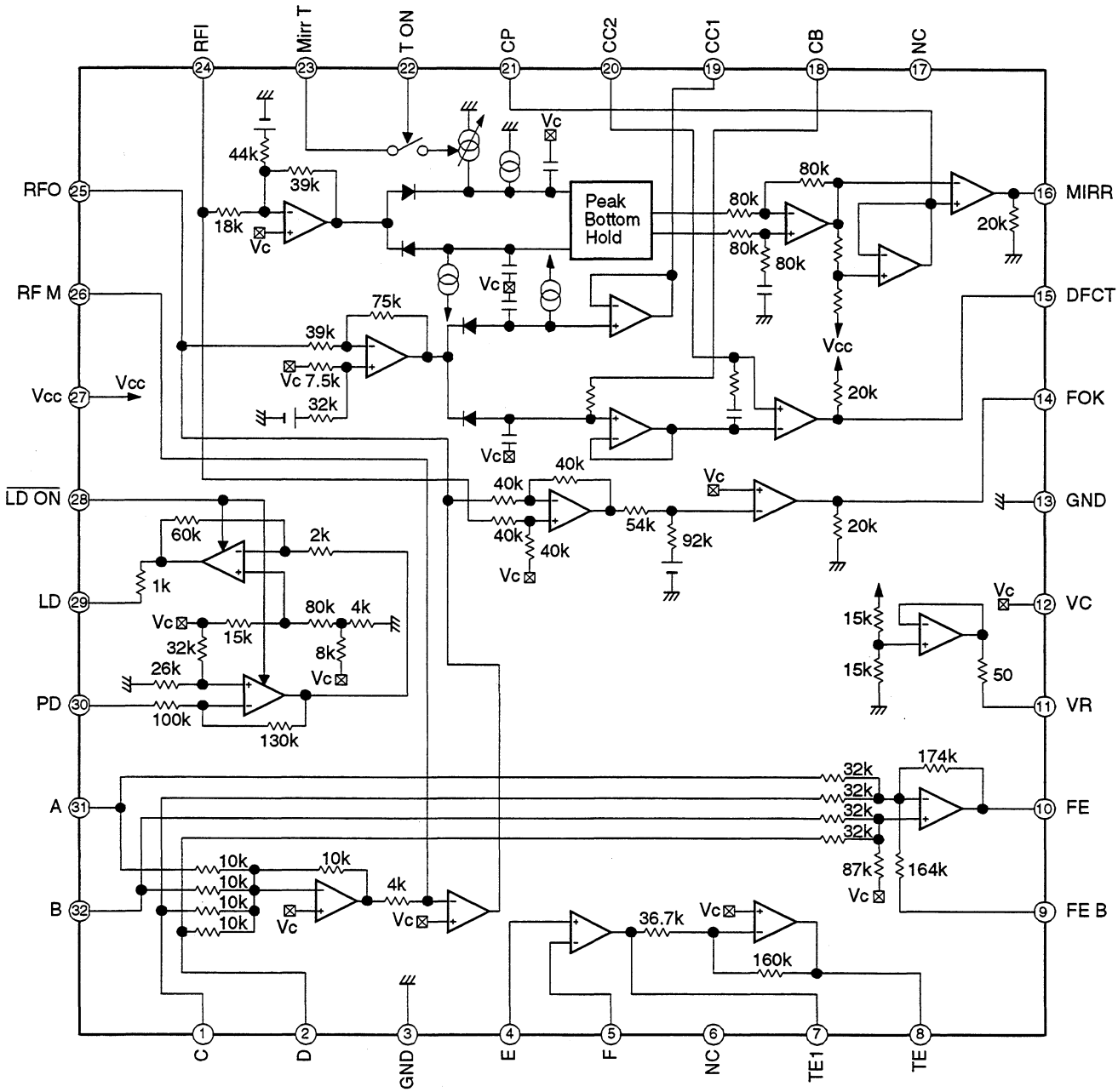
No.	Name	Function
1	OUT1-A	Driver CH1 output terminal.
2	OUT1-B	Driver CH1 output terminal.
3	PRE-OUT1	CH1 previous-stage amplifier output terminal.
4	IN1 (-)	CH1 previous-stage amplifier reverse input terminal.
5	IN1 (+)	CH1 previous-stage amplifier non-reverse input terminal.
6	REG-B	External Tr base connection terminal.
7	REG-OUT	Constant-voltage output (external Tr collector connection).
8	BIAS-IN	Bias input terminal.
9	MUTE	Mute control terminal.
10	IN2 (+)	CH2 previous-stage amplifier non-reverse input terminal.
11	IN2 (-)	CH2 previous-stage amplifier reverse input terminal.
12	PRE-OUT2	CH2 Previous-stage amplifier output terminal.
13	OUT2-B	Driver CH2 output terminal.
14	OUT2-A	Driver CH2 output terminal.

No.	Name	Function
15	GND	Substraight GND.
16	OUT3-A	Driver CH3 output terminal.
17	OUT3-B	Driver CH3 output terminal.
18	PRE-OUT3	CH3 previous-stage amplifier output terminal.
19	IN3 (-)	CH3 previous-stage amplifier reverse input terminal.
20	IN3 (+)	CH3 previous-stage amplifier non-reverse input terminal.
21	VCC	VCC
22	VCC	VCC
23	IN4 (+)	CH4 previous-stage amplifier non-reverse input terminal.
24	IN4 (-)	CH4 previous-stage amplifier reverse input terminal.
25	PRE-OUT4	CH4 previous-stage amplifier output terminal.
26	OUT4-B	Driver CH4 output terminal.
27	OUT4-A	Driver CH4 output terminal.
28	GND	Substraight GND.

■ CXA2521AQ (DVD MAIN ASSY : IC901)

● RF AMP

● Block Diagram



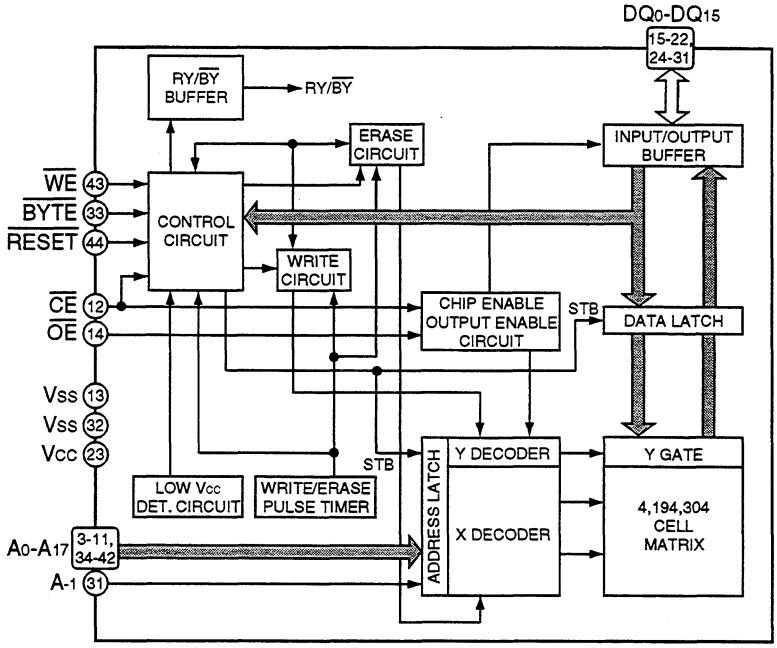
● Pin Function

No.	Name	I/O	Function
1	C	I	Input terminal for the RF summing amplifier and focus error amplifier.
2	D	I	Input terminal for the RF summing amplifier and focus error amplifier.
3	GND	-	Grounding terminal.
4	E	I	Input terminal for the tracking error amplifier.
5	F	I	Input terminal for the tracking error amplifier.
6	NC	-	Open on the circuit.
7	TE1	O	Output for the tracking error amplifier and input terminal for the tracking error drive .
8	TE	O	Output terminal for the tracking error amplifier.
9	FE B	I	Focus bias adjusting terminal for the focus amplifier.
10	FE	O	Output terminal for the focus error amplifier.
11	VR	O	DC voltage output terminal for (Vcc + GND)/2.
12	VC	I	Mid-point voltage input terminal for VC.
13	GND	-	Grounding terminal.
14	FOK	O	Output terminal for the FOK comparator.
15	DFCT	O	Output terminal for the DEFECT comparator.
16	Mirr	O	Output terminal for the mirror comparator.
17	NC	-	Open on the circuit.
18	CB	I	Connection terminal for the DEFECT Bottom Hold capacitor.
19	CC1	O	Output terminal for DEFECT Bottom Hold.
20	CC2	I	Input terminal to which combined capacity of output from DEFECT Bottom Hold is input.
21	CP	I	Connection terminal for the Mirror Hold capacitor and non-reverse input terminal for the mirror comparator.
22	T ON	I	Time constant switching terminal for Peak Hold. Connecting the terminal to Vcc enables adjustment of time constant. Connecting the terminal to GND fixes time constant.
23	Mirr	I	Time constant adjusting terminal for Peak Hold. Time constant is set to that adjusted when Terminal 22 was turned to ON.
24	RFI	I	Input terminal to which combined capacity of output from the RF summing amplifier is input.
25	RFO	O	Output terminal for RF signal. The value of resistor connected between Terminals 25 and 26 determines the low-frequency gain of the RF drive amplifier.
26	RF M	I	Input terminal on the reverse side for the RF drive amplifier.
27	Vcc	-	Vcc pin.
28	$\overline{\text{LD ON}}$	I	APC amplifier ON/OFF switching terminal. Connecting the terminal to Vcc turns the amplifier to OFF. Connecting the terminal to GNC turns the amplifier to ON.
29	LD	O	Output terminal for the APC amplifier.
30	PD	I	Input terminal for the APC amplifier.
31	A	I	Input terminal for the RF summing amplifier and focus error amplifier.
32	B	I	Input terminal for the RF summing amplifier and focus error amplifier.

■ MBM29F400TA-70PF (VYW1515) (DVD MAIN ASSY : IC1030)

● 4M bit FLASH MEMORY

● Block Diagram



● Pin Function

No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	N.C.	Non connection	23	V_{CC}	Power supply (+5.0V ± 10% or ± 5%)
2	RY/$\overline{BY}$	Ready/Buzy output	24	DQ_4	Data input/output
3	A_{17}	Address input	25	DQ_{12}	
4	A_7		26	DQ_5	
5	A_6		27	DQ_{13}	
6	A_5		28	DQ_6	
7	A_4		29	DQ_{14}	
8	A_3		30	DQ_7	
9	A_2		31	DQ_{15}/A_{-1}	Data input / output / address input
10	A_1		32	V_{SS}	Ground
11	A_0		33	$\overline{BYTE}$	Mode select of 8 bit and 16 bit
12	$\overline{CE}$	Chip enable	34	A_{16}	Address input
13	V_{SS}	Ground	35	A_{15}	
14	$\overline{OE}$	Output enable	36	A_{14}	
15	DQ_0	Data input /output	37	A_{13}	
16	DQ_8		38	A_{12}	
17	DQ_1		39	A_{11}	
18	DQ_9		40	A_{10}	
19	DQ_2		41	A_9	
20	DQ_{10}		42	A_8	
21	DQ_3		43	$\overline{WE}$	Write enable
22	DQ_{11}		44	$\overline{RESET}$	Hard ware reset